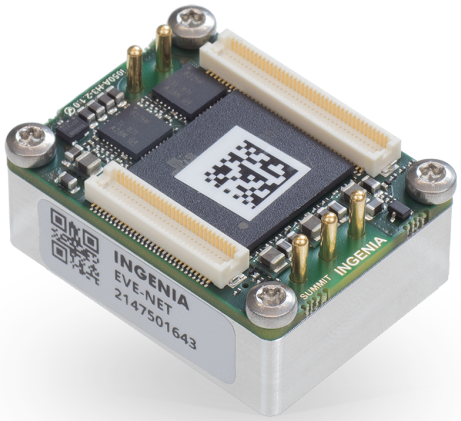
# Everest NET - Product Manual

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*For the most up to date information visit the online manual.*



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passion for motion

# 1. Table of Contents

# 2. General Information

## 2.1. Manual revision history

| Revision | Release Date | Changes | PDF |
|---|---|---|---|
| v1 | 2019-4-12 | Initial version | Export as pdf |

For the most up to date information use the online Product Manual.

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# 3. Safety Information

## 3.1. About this manual

Read carefully this chapter to raise your awareness of potential risks and hazards when working with the Everest NET Servo Drive.

To ensure maximum safety in operating the Everest NET Servo Drive, it is essential to follow the procedures included in this guide. This information is provided to protect users and their working area when using the Everest NET Servo Drive, as well as other hardware that may be connected to it. Please read this chapter carefully before starting the installation process.

## 3.2. Warnings

The following statements should be considered to avoid serious injury to those individuals performing the procedures and/or damage to the equipment:

- To prevent the formation of electric arcs, as well as dangers to personnel and electrical contacts, never connect/disconnect the Everest NET Servo Drive while the power supply is on.
- Disconnect the Everest Servo Drive from all power sources before proceeding with any possible wiring change.
- After turning off the power and disconnecting the equipment power source, wait at least 10 seconds before touching any parts of the controller that are electrically charged or hot.

## 3.3. Precautions

The following statements should be considered to avoid serious injury to those individuals performing the procedures and/or damage to the equipment:

- The Everest Servo NET Drive components temperature may exceed 100 ºC during operation.
- Some components become electrically charged during and after operation.
- The power supply connected to this controller should comply with the parameters specified in this document.
- When connecting the Everest Servo NET Drive to an approved power source, do so through a line that is separate from any possible dangerous voltages, using the necessary insulation in accordance with safety standards.
- High-performance motion control equipment can move rapidly with very high forces. Unexpected motion may occur especially during product commissioning. Keep clear of any operational machinery and never touch them while they are working.
- Do not make any connections to any internal circuitry. Only connections to designated connectors are allowed.
- All service and maintenance must be performed by qualified personnel.
- Before turning on the Everest Servo NET Drive, check that all safety precautions have been followed, as well as the installation procedures.

# 4. Product Description

Everest NET is a high power, highly-integrated, digital servo drive intended to be plugged or soldered to an application-specific daughter board. The drive features best-in-class energy efficiency thanks to its state of the art power stage, and can be easily configured with Ingenia's free-to-download software MotionLab 3.

Everest NET is enabled with **EtherCAT** and **CANopen** communications.

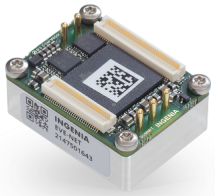
**Main features:**

- Ultra-small footprint
- 80 $V_{DC}$, 30 $A_{RMS}$ continuous
- Up to 99% efficiency
- Up to 75 kHz current loop, 25 kHz servo loops
- 10 kHz ~ 100 kHz PWM frequency
- 16 bit ADC with VGA for current sensing
- Supports Halls, Quadrature encoder, SSI and BiSS-C
- Up to 4 simultaneous feedback sources
- Full voltage, current and temperature protections

**Typical applications:**

- Collaborative robot joints
- Robotic exoskeletons
- Wearable robots
- AGVs
- UAVs
- Industrial highly integrated servomotors
- Smart motors
- Battery-powered and e-Mobility
- Low inductance motors

## 4.1. Part numbering

| Product | Ordering part number | Status | Image |
|---|---|---|---|
| **Everest NET**<br>Pluggable servo drive with EtherCAT & CANopen communication. | EVE-NET | PRE-PROD. |  |

For applications not requiring CANopen or EtherCAT, please see **Everest CORE**.

For applications requiring a ready-to-go product, please see Everest XCR.

### 4.2. Specifications

| **Part number →** | **EVE-NET** |
|---|---|
| **Electrical and power specifications** | |
| **Minimum DC bus supply voltage** | 8 $V_{DC}$ |
| **Maximum DC bus supply voltage** | 80 $V_{DC}$ (continuous)<br>85 $V_{DC}$ (peak 100 ms) |
| **Recommended power supply voltage range** | 12 $V_{DC}$ ~ 72 $V_{DC}$<br>This voltage range ensures a safety margin including power supply tolerances and regulation during acceleration and braking. |
| **Internal drive DC bus capacitance** | 6 µF |
| **Logic supply voltage** | 4.9 $V_{DC}$ ~ 5.1 $V_{DC}$ |
| **Nominal phase continuous current (RMS)** | 30 A |
| **Maximum phase peak current (RMS)** | 60 A @ 3 sec<br>Active current limiting based on power stage and motor temperature. |
| **Efficiency** | Up to 99% @ 20 kHz, 80 V, 30 A |
| **Bus voltage utilisation** | > 97% @ 20 kHz, 80 V, voltage mode, no load |
| **Motion control specifications** | |
| **Standby logic supply consumption** | ≤ 3.3 W<br>Measured with an active Ethernet communication, and commutation turned OFF.<br>The measurement includes 150 mW corresponding to the Ethernet magnetics, not included in the Everest NET. |
| **Supported motor types** | • Rotary brushless (SVPWM and Trapezoidal)<br>• Rotary brushed (DC) |
| **Power stage PWM frequency (configurable)** | 10 kHz, 20 kHz (default), 50 kHz & 100 kHz |
| **Current sensing** | 16 bit ADC resolution. Accuracy is ±2% full scale. |

| | |
|---|---|
| **Current sense resolution (configurable)** | Current gain is configurable in 4 ranges:<br>• 2.475 mA/count<br>• 1.352 mA/count<br>• 0.570 mA/count<br>• 0.379 mA/count |
| **Current sense ranges (configurable)** | Current ranges for the 4 configurable current gains:<br>• ±81.1 A<br>• ±44.3 A<br>• ±18.7 A<br>• ±12.4 A |
| **Max. Current loop frequency** | 75 kHz |
| **Max. servo loops frequency (position & velocity)** | 25 kHz @ 75 kHz current loop |
| **Feedbacks** | • Digital Halls<br>• Quadrature / Incremental encoder<br>• Absolute Encoder: up to 2 at the same time, combining any of the following:<br>  • BiSS-C (up to 2 in daisy chain topology)<br>  • SSI<br>*Only a specific subset of absolute encoders are supported. Contact Ingenia for further information. |
| **Supported target sources** | Network communication (EtherCAT or CANopen) |
| **Control modes** | • Cyclic Synchronous Position<br>• Cyclic Synchronous Velocity<br>• Cyclic Synchronous Current<br>• Profile Position (trapezoidal & s-curves)<br>• Profile Velocity<br>• Interpolated Position (P, PT, PVT)<br>• Homing |

| **Inputs/outputs and protections** | |
|---|---|
| **Inputs and outputs** | 4 x non-isolated single-ended digital inputs - 3.3 V logic level. Can be configured as:<br>• General purpose<br>• Positive or negative homing switch<br>• Positive or negative limit switch<br>• Quick stop input<br>4 x non-isolated single-ended digital outputs - 3.3 V logic level, 3 mA max. sink / source current. Can be configured as:<br>• General purpose<br>• Operation enabled event flag<br>• External shunt braking resistor driving signal<br>1 x ±3.3 V ,16-bit, differential analog input for load cells or torque sensors. Can be read by the Master to close a torque loop. |
| **Shunt braking resistor output** | Configurable over any of the digital outputs (see above).<br>Enabling this function would require an external transistor or power driver. |
| **Motor brake output** | Dedicated, PWM capable, 3.3 V digital output for driving a mechanical brake. Turn-on and turn-off times are configurable.<br>Enabling this function would require an external transistor or power driver. |
| **Safe Torque OFF inputs** | 2 x dedicated, non-isolated STO digital inputs (3.3 V and 5 V tolerant). |
| **Motor temperature input** | 1 x dedicated, 5 V, 12-bit, single-ended analog input for measuring motor temperature. |
| **Protections** | • Hardcoded / hardwired Drive protections:<br>  • Automatic current derating on voltage, current and temperature<br>  • Short-circuit Phase to DC bus<br>  • Short-circuit Phase to Phase<br>  • Short-circuit Phase to GND<br>• Configurable protections:<br>  • DC bus over-voltage<br>  • DC bus under-voltage<br>  • Drive over-temperature<br>  • Drive under-temperature<br>  • Motor over-temperature (requires external sensor)<br>  • Current overload ($I^2t$). Configurable up to Drive limits<br>  • Voltage mode over-current (with a closed current loop, protection effectiveness depends on the PID).<br>• Motion Control protections:<br>  • Halls sequence / combination error (Pending implementation)<br>  • Limit switches<br>  • Position following error<br>  • Velocity / Position out of limits |

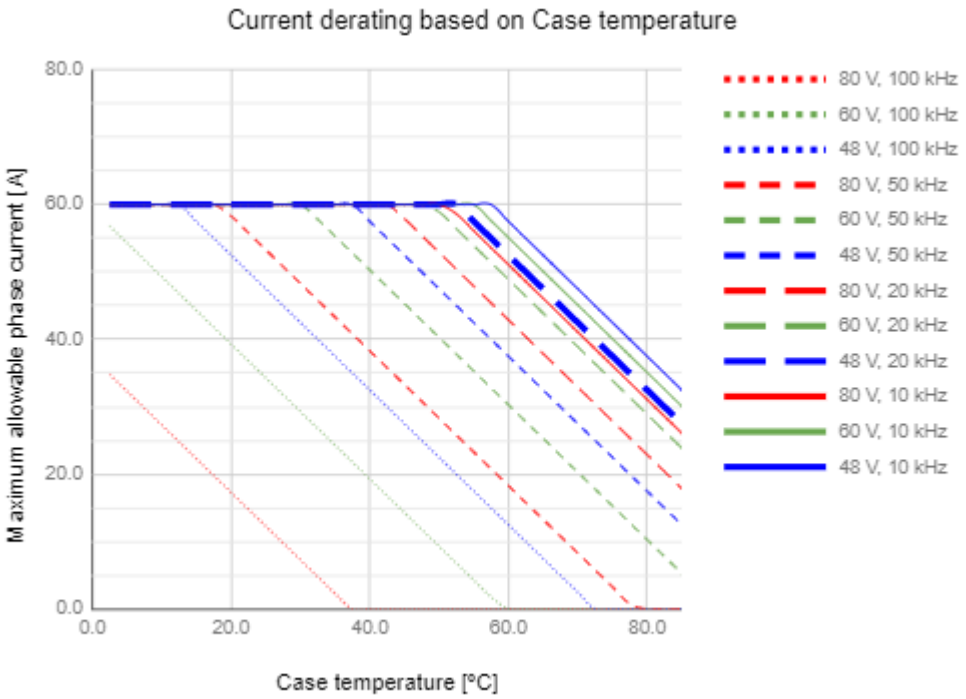
| | |
|---|---|
| **Communications** | |
| **CANopen (by default)** | CiA-301, CiA-303, CiA-305, CiA-306 and CiA-402 (4.0) compliant.<br>Note: when configured as CANopen the Ethernet ports can still be used to configure the drive. |
| **EtherCAT (software selectable)** | CANopen over EtherCAT (CoE)<br>File over EtherCAT (FoE)<br>Ethernet over EtherCAT (EoE) |
| **Environmental conditions** | |
| **Aluminium case** | Yes (connectors side open) |
| **Case temperature** | Operation:<br>• -40 ºC to +60 ºC at full current<br>• +60 ºC to +85 ºC with derated current<br>For further information, see Thermal Specifications below.<br>Storage:<br>• -40 ºC to +100 ºC |
| **Maximum humidity** | 5% ~ 85% non-condensing |
| **Mechanical specifications** | |
| **Horizontal dimensions** | 34.5 mm x 26 mm |
| **Height** | 15 mm (including 3 mm board-to-board distance)<br>17 mm (including full length of the power pins) |
| **Weight** | 24 gr |
| **Certifications** | |
| **Certification** | CE, RoHS<br>STO SIL3 (certification pending) |

### 4.3. Thermal specifications

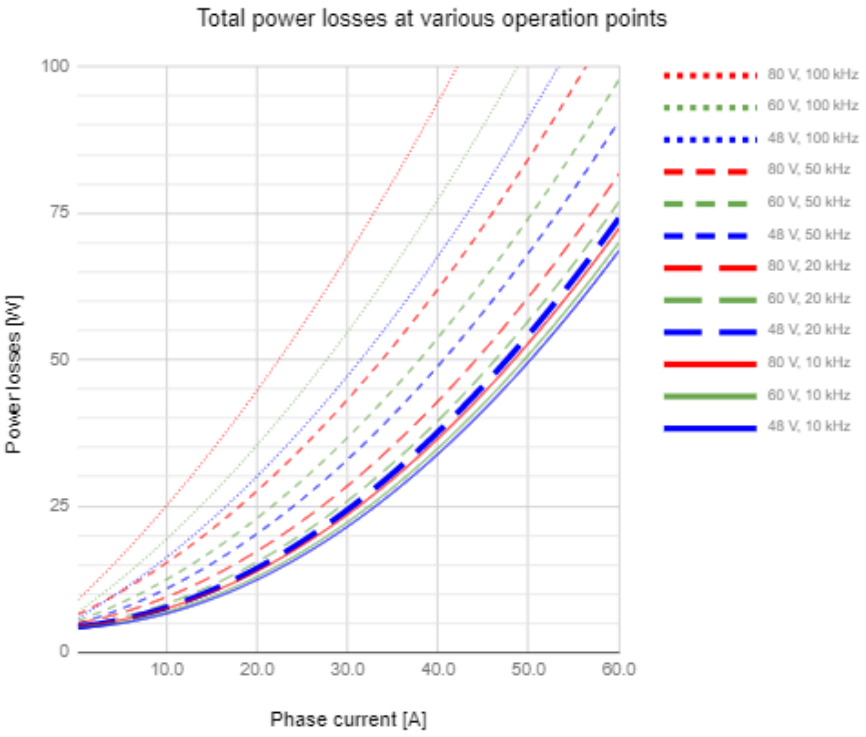
Thermal performance of Everest NET is specified as function of the **temperature measured in its aluminium case**, the **DC bus voltage** and the **PWM commutation frequency**. This 3 parameters could ultimately determine the maximum continuous current the Everest NET can output, provided that an **active derating** algorithm will be continuously protecting it from thermal over-stress. Notice that PWM commutation frequency cannot be changed dynamically, but pre-selected to match the application needs: most probably 10 kHz will be selected for highest current at a given temperature (be aware that selecting this frequency may cause audible noise), but 100 kHz will be preferred to control a low inductance motor.

The following figure show the maximum phase current at different case temperatures and DC bus voltages. Here **current is expressed in RMS**. To obtain the equivalent current in amplitude just multiply it by √2 .

To ensure a proper performance of Everest NET, the **case temperature must be held always below 85 ºC ($T_{c\text{-}max}$ = 85 ºC).**



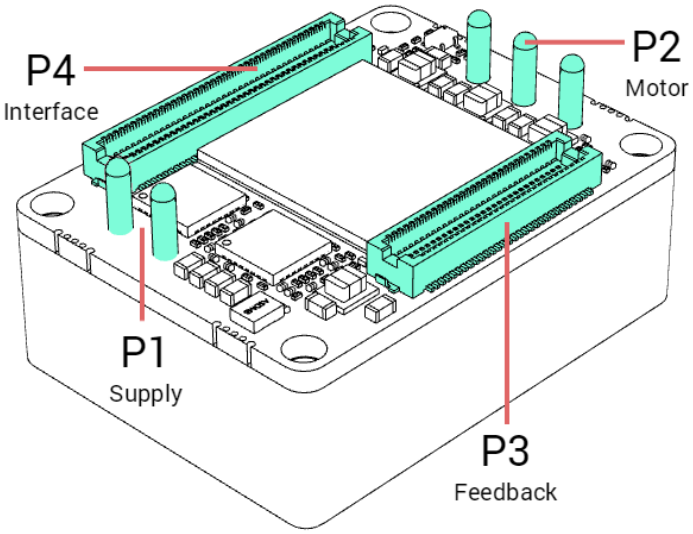

Following figure show the theoretical **power losses** at different operating points.



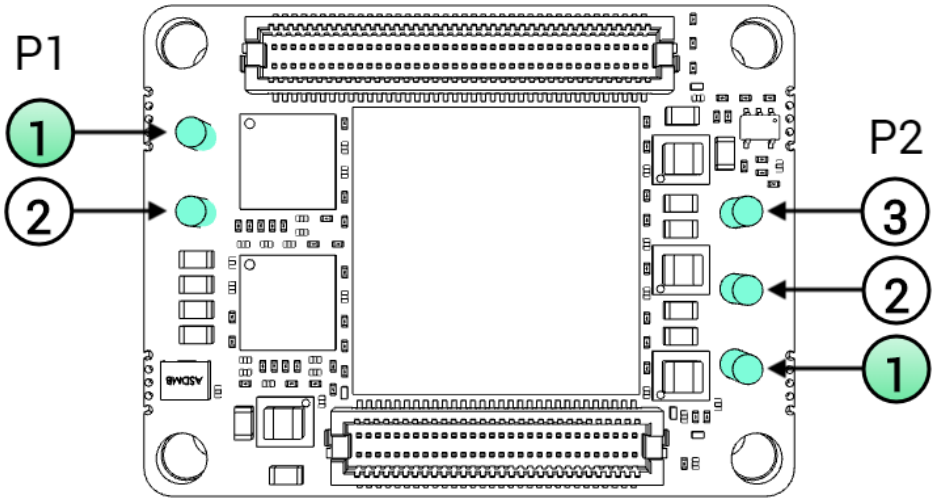

Take a look to the Thermal Dissipation section below to learn how to dimension a heatsink to allow Everest NET reaching a target current under an specific ambient temperature.

# 5. Pinout

## 5.1. Connectors Overview




## 5.2. P1 and P2 Power pins



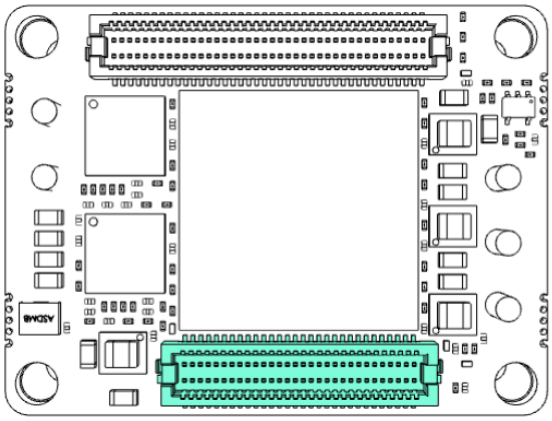

| **P1 Supply Power pins** | | | |
|---|---|---|---|
| **Pin** | **Name** | **Type** | **Function** |
| 1 | POW_SUP | Power | Power supply positive (DC bus). |
| 2 | GND_P | | Power supply negative (Power Ground). |
| Chassis | PE | | Protective Earth connected to driver housing and fixing M2.5 threads. |

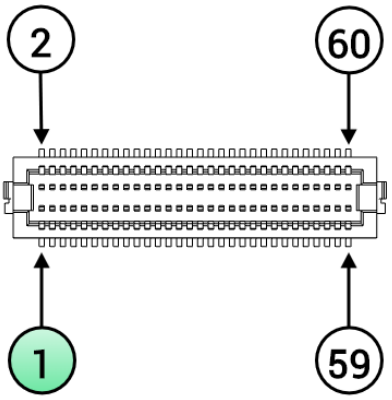
| **P2 Motor Power pins** | | | |
|---|---|---|---|
| **Pin** | **Name** | **Type** | **Function** |
| 1 | PH_A | Power | Motor phase A for 3-phase motors, positive for DC motors. |
| 2 | PH_B | | Motor phase B for 3-phase motors, negative for DC motors. |
| 3 | PH_C | | Motor phase C for 3-phase motors (do not connect for DC motors). |
| Chassis | PE | | Protective Earth connected to driver housing and fixing M2.5 threads. |

| **Everest NET power pins** | **Recommended mating contact** | **Description** |
|---|---|---|
| | **Up to 11.2 $A_{RMS}$ rated motors** | |
| Ø 1.52 mm, 4 mm pitch, gold plated power pins. |  | Beryllium copper TH pin receptacle. Gold plated. |
| | Mill-Max 9372-0-15-15-23-27-10-0 | |
| | **> 11.2 $A_{RMS}$ rated motors** | |
| | Direct solder to PCB. TH pad with min. hole Ø 1.63 mm. Ensure PCB track are wide enough to withstand the target current. | |
| **Chassis (aluminium body)** | | |
| 3 mm board-to-board height spacers. |  | Surface-mount tinned steel round spacer, Ø 2.7 mm internal, Ø 5.1 mm external, 3 mm board-to-board height. |
| | Wurth Electronics 9774030951R | |

### 5.3. P3 Feedback connector

The pinout of the Feedback connector is exactly the same for for Everest NET (EVE_NET) and Everest CORE (EVE_CORE) although the **position of the connector is different**.






**P3 Feedback connector**

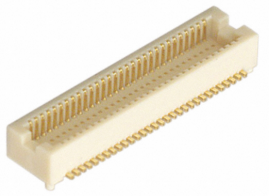
| # | Signal name | Description | Type | # | Signal name | Description | Type |
|---|---|---|---|---|---|---|---|
| **1** | GND_A | Analog Ground. Do not connect to GND_D directly, use a ferrite bead or 1 Ω resistor in between. | Power | **2** | GND_A | Analog Ground. Do not connect to GND_D directly, use a ferrite bead or 1 Ω resistor in between. | Power |
| **3** | DNC | Reserved. Do not connect (leave floating). | - | **4** | AN1_P | Analog input for torque sensing. | 16 bit differential analog input |
| **5** | DNC | | | **6** | AN1_N | | |
| **7** | DNC | | | **8** | DNC | Reserved. Do not connect (leave floating). | - |
| **9** | DNC | | | **10** | DNC | | |
| **11** | DNC | | | **12** | DNC | | |
| **13** | MOTOR_TEMP | Motor temperature sensor input. 0 V to 5 V level high impedance input. | 12 bit single-ended analog input | **14** | DNC | | |
| **15** | GND_D | Digital signal Ground. | Power | **16** | NC | Internally not connected. Recommended to leave them unconnected. | |
| **17** | HALL_1 | Digital hall 1. | Input | **18** | NC | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **19** | HALL_2 | Digital hall 2. | | **20** | GND_A | Analog Ground. Do not connect to GND_D directly, use a ferrite bead or 1 Ω resistor in between. | Power |
| **21** | HALL_3 | Digital hall 3. | | **22** | GND_D | Digital signal Ground. | |
| **23** | CLL | Reserved. Must be tied or pulled-down to GND_D. | - | **24** | DIG_ENC_1A | Digital encoder 1 A. | Input |
| **25** | CHL | Reserved. Must be tied or pulled-up to 3.3 V. | | **26** | DIG_ENC_1B | Digital encoder 1 B. | |
| **27** | CLL | Reserved. Must be tied or pulled-down to GND_D. | | **28** | DIG_ENC_1Z | Digital encoder 1 Index. | |
| **29** | CHL | Reserved. Must be tied or pulled-up to 3.3 V. | | **30** | DIG_ENC_2A | Digital encoder 2 A. | |
| **31** | DNC | Reserved. Do not connect (leave floating). | | **32** | DIG_ENC_2B | Digital encoder 2 B. | |
| **33** | DNC | | | **34** | DIG_ENC_2Z | Digital encoder 2 Index. | |
| **35** | DNC | | | **36** | GND_D | Digital signal Ground. | Power |
| **37** | DNC | | | **38** | ABSENC1_CLK | Clock output for Absolute Encoder 1. | Output |
| **39** | DNC | | | **40** | ABSENC1_DATA | Data input for Absolute Encoder 1 (supports SSI or up to 2 BiSS-C encoders connected in daisy chain topology). | Input |
| **41** | DNC | | | **42** | DNC | Reserved. Do not connect (leave floating). | - |
| **43** | DNC | | | **44** | GND_D | Digital signal Ground. | Power |
| **45** | DNC | | | **46** | DNC | Reserved. Do not connect (leave floating). | - |
| **47** | DNC | | | **48** | DNC | | |
| **49** | DNC | | | **50** | DNC | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **51** | DNC | | | **52** | DNC | | |
| **53** | DNC | | | **54** | DNC | | |
| **55** | DNC | | | **56** | DNC | | |
| **57** | DNC | | | **58** | DNC | | |
| **59** | GND_D | Digital signal Ground. | Power | **60** | GND_D | Digital signal Ground. | Power |

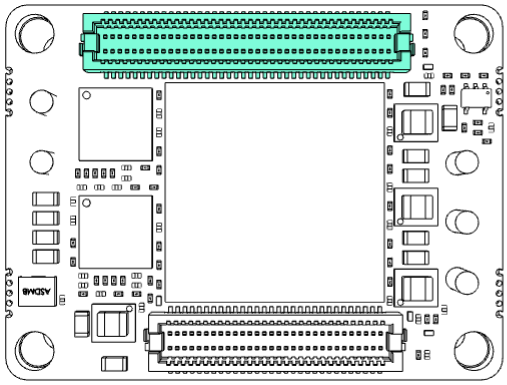
**Notes and naming conventions:**

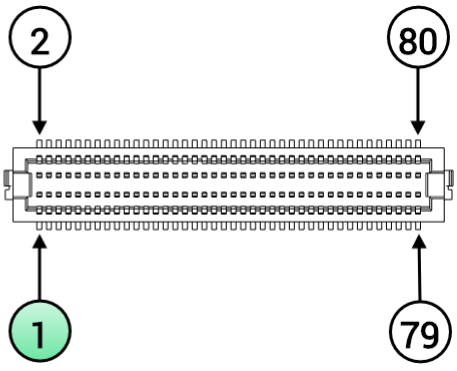
- All pins are tolerant to 3.3 V unless otherwise noted.
- "_P" and "_N" indicates positive and negative of differential signals
- "\" Indicates inverted (active low) signal
- "NC" means Not Connected. Pins marked with NC can be tied to GND or 3.3 V, but best practice is to leave them unconnected.
- "DNC" means Do Not Connect. Pins marked with DNC must not be tied to any driving voltage, including GND or 3.3 V.
- "CLL" means Connect to Low Level. Pins marked with CLL must be tied or pulled-down to 0 V.
- "CHL" means Connect to High Level. Pins marked with CHL must be tied or pulled-up to 3.3 V.

| Manufacturer | Everest NET connector | Required mating connector | Description |
|---|---|---|---|
| Hirose Electric |  |  | 60-pin mezzanine stacking board connector. 0.5 mm pitch. Center strip, gold-plated surface mount contacts. 3 mm stacking height. |
| | DF12(3.0)-60DP-0.5V(86) | DF12(3.0)-60DS-0.5V(86) | |

## 5.4. P4 Everest NET Interface connector

Although using the same physical connector as **Everest CORE** (EVE-CORE), position and pinout is different in Everest NET (EVE-NET).





| **P4 Everest NET Interface connector** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **#** | **Signal name** | **Description** | **Type** | **#** | **Signal name** | **Description** | **Type** |
| **1** | 3.3V_REF | 3.3 V voltage reference output with sink/source capability up to ±10 mA. An excessive current demand or noise coupled to this pin can cause a loss of performance or even malfunction of Everest NET: route by following the best layout practices. | Power output | **2** | DNC | Reserved. Do not connect (leave floating). | - |
| **3** | GND_A | Analog Ground. Do not connect to GND_D directly, use a ferrite bead or 1 Ω resistor in between. | Power | **4** | 1.65V_REF | 1.65 V voltage reference output with sink/source capability up to ±10 mA. An excessive current demand or noise coupled to this pin can cause a loss of performance or even malfunction of Everest NET: route by following the best layout practices. | Power output |
| **5** | GND_D | Digital signal Ground. | | **6** | GND_D | Digital signal Ground. | Power |
| **7** | 5V_D | 5 V, 1 A continuous logic supply input. Must be low ripple and ensure ±2% regulation tolerance or less. All four 5V_D pins must be connected. It is advised to provide at least 1.2 A input current if pins 13 or 14 (3.3V_D) are used to drive external circuits. | Power input | **8** | 5V_D | 5 V, 1 A continuous logic supply input. Must be low ripple and ensure ±2% regulation tolerance or less. All four 5V_D pins must be connected. It is advised to provide at least 1.2 A input current if pins 13 or 14 (3.3V_D) are used to drive external circuits. | Power input |
| **9** | 5V_D | | | **10** | 5V_D | | |
| **11** | GND_D | Digital signal Ground. | Power | **12** | GND_D | Digital signal Ground. | Power |
| **13** | MAGNETICS_CT | Dedicated voltage output for the EtherCAT magnetics center tap. Do not connect this pin to other voltage source or load other than the center tap of the EtherCAT transformers. Do not connect to pin 14. | Power output | **14** | 3.3V_D | 3.3 V, 250 mA max. output to supply peripherals. An excessive current demand on this pin could cause failure or even permanent damage to the Everest NET. | Power output |
| **15** | GND_D | Digital signal Ground. | Power | **16** | GND_D | Digital signal Ground. | Power |
| **17** | GPO4 | Digital Output 4. | Output | **18** | GPI1 | Digital Input 1. | Input |
| **19** | GPI2 | Digital Input 2. | Input | **20** | GPI3 | Digital Input 3. | |

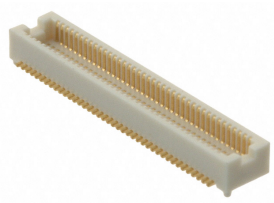
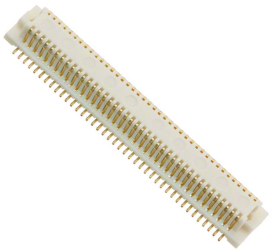
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **21** | DNC | Reserved. Do not connect (leave floating). | - | **22** | DNC | Reserved. Do not connect (leave floating). | - |
| **23** | DNC | | | **24** | ABSENC2_CLK | Clock output for Absolute Encoder 2. | Output |
| **25** | ABSENC2_DATA | Data input for Absolute Encoder 2 (supports SSI only) | Input | **26** | DNC | Reserved. Do not connect (leave floating). | - |
| **27** | DNC | Reserved. Do not connect (leave floating). | - | **28** | DNC | | |
| **29** | GPO1 | Digital Output 1. | Output | **30** | GPO2 | Digital Output 2. | Output |
| **31** | GPO3 | Digital Output 3. | | **32** | GPI4 | Digital Input 4. | Input |
| **33** | \STO1 | Safe Torque Off input 1 (non-isolated). Both \STO1 and \STO2 must be high-level (3.3 V and 5 V level compatible) to allow operation of the motor. Holding different logic states (STO1 ≠ STO2) for more than 1s will cause a latching fault. | Input | **34** | \STO2 | Safe Torque Off input 2 (non-isolated). Both \STO1 and \STO2 must be high-level (3.3 V and 5 V level compatible) to allow operation of the motor. Holding different logic states (STO1 ≠ STO2) for more than 1s will cause a latching fault. | |
| **35** | GND_D | Digital signal Ground. | Power | **36** | FAULT_SIGNAL | Fault state signalling output. Can directly drive a (typically) red LED anode at 3.3 V up to 3 mA. | Output |
| **37** | DNC | Reserved. Do not connect (leave floating). | - | **38** | GND_D | Digital signal Ground. | Power |
| **39** | DNC | | | **40** | DNC | Reserved. Do not connect (leave floating). | - |
| **41** | PWM_BRAKE | PWM output for driving a mechanical brake. Configurable up to 20 kHz. High level indicates the motor is free to move. | Output | **42** | DNC | | |
| **43** | DNC | Reserved. Do not connect (leave floating). | - | **44** | DNC | | |
| **45** | DNC | | | **46** | GND_D | Digital signal Ground. | Power |
| **47** | DNC | | | **48** | DNC | Reserved. Do not connect (leave floating). | - |
| **49** | DNC | | | **50** | DNC | | |
| **51** | DNC | | | **52** | DNC | | |
| **53** | DNC | | | **54** | DNC | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **55** | CAN_TX | 3.3 V TTL-levels Transmit pin of CAN data frame. Requires an external transceiver to shift into CAN physical layer. | Output | **56** | DNC | | |
| **57** | CAN_RX | 3.3 V TTL-levels Receive pin of CAN data frame. Requires an external transceiver to shift into CAN physical layer. | Input | **58** | DNC | | |
| **59** | GND_D | Digital signal Ground. | Power | **60** | GND_D | Digital signal Ground. | Power |
| **61** | DNC | Reserved. Do not connect (leave floating). | - | **62** | DNC | Reserved. Do not connect (leave floating). | - |
| **63** | DNC | | | **64** | ECAT_CAN_ERR | State machine ERROR red LED for EtherCAT and CANopen. Can directly drive a red LED anode at 3.3 V up to 3 mA. | Output |
| **65** | ECAT_CAN_RUN | State-machine RUN green LED output for EtherCAT and CANopen. Can directly drive a green LED anode at 3.3 V up to 3 mA. | Output | **66** | DNC | Reserved. Do not connect (leave floating). | - |
| **67** | \ETH0_LED_LINK | Ethernet Port 0 Link signalling. Must be connected to a high impedance or be buffered to drive a (typically) green LED. | | **68** | \ETH1_LED_LINK | Ethernet Port 1 Link signalling. Must be connected to a high impedance or be buffered to drive a (typically) green LED. | Output |
| **69** | GND_D | Digital signal Ground. | Power | **70** | GND_D | Digital signal Ground. | Power |
| **71** | PHY0_TX_P | Port 0 Ethernet physical layer differential pairs. 50 Ω termination resistors are included, but magnetics with center tap connected to 3.3V_D (pins 13 and 14) must be added externally. | I/O | **72** | PHY1_TX_P | Port 1 Ethernet physical layer differential pairs. 50 Ω termination resistors are included, but magnetics with center tap connected to 3.3V_D (pins 13 and 14) must be added externally. | I/O |
| **73** | PHY0_TX_N | | | **74** | PHY1_TX_N | | |
| **75** | PHY0_RX_P | | | **76** | PHY1_RX_P | | |
| **77** | PHY0_RX_N | | | **78** | PHY1_RX_N | | |
| **79** | GND_D | Digital signal Ground. | Power | **80** | GND_D | Digital signal Ground. | Power |

**Notes and naming conventions:**

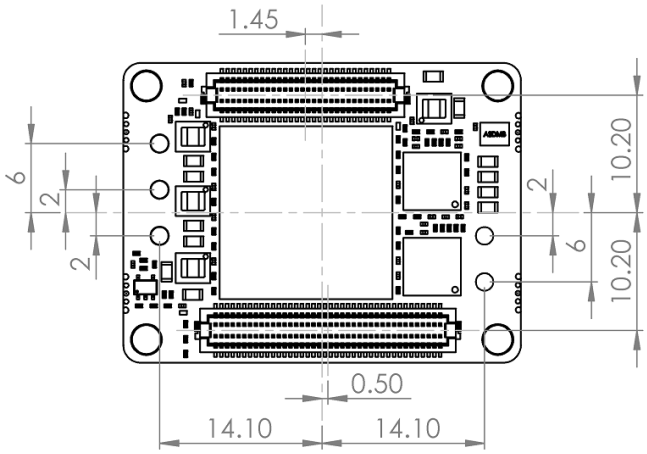
- All pins are tolerant to 3.3 V unless otherwise noted.
- "_P" and "_N" indicates positive and negative of differential signals
- "\" Indicates inverted (active low) signal
- "NC" means Not Connected. Pins marked with NC can be tied to GND or 3.3 V, but best practice is to leave them unconnected.

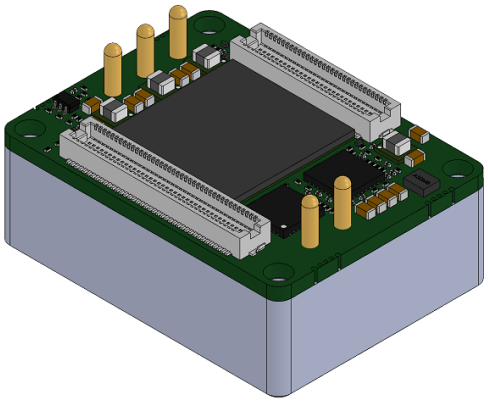
- "DNC" means Do Not Connect. Pins marked with DNC must not be tied to any driving voltage, including GND or 3.3 V.

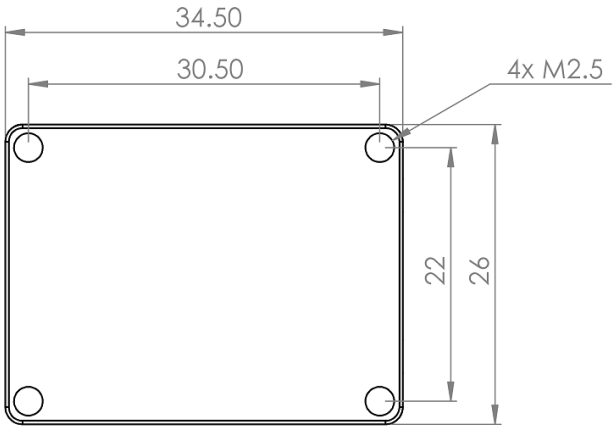
| Manufacturer | Everest NET connector | Required mating connector | Description |
|---|---|---|---|
| Hirose Electric |  |  | 80-pin mezzanine stacking board connector. 0.5 mm pitch. Center strip, gold-plated surface mount contacts. 3 mm stacking height. |
| | DF12(3.0)-80DP-0.5V(86) | DF12(3.0)-80DS-0.5V(86) | |

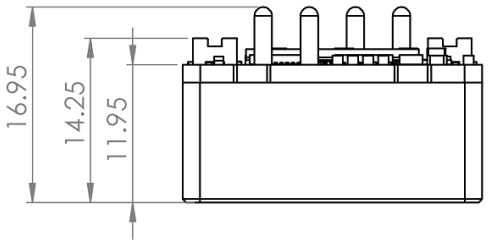
# 6. Dimensions

All dimensions are in **mm**. All tolerances **≤ ±0.2 mm**






**3D Model**
For further detail, download the STEP model.

# 7. Application Guide

## 7.1. Scope and Architecture

Everest NET is a highly integrated universal servo drive. This means that a lot of features are available, although only a set of them might be required in an specific application. This set of features can be activated by populating an interface board with simple components, like transceivers, voltage dividers or filters. However, due to its miniature scale and power density, setting the required electronics might require specific design practices. This chapter is intended to provide advice on this practices, from thermal dissipation to PCB layout.

Whenever designing an interface board for Everest NET is out of the scope, please consider Everest XCR as a ready-to-go alternative.

### 7.1.1. Parts of an Everest NET integration solution

**Everest NET:** includes the Motion Controller, the Power Stage and the Communications Controller.

**Interface board:** should include the adaptor electronics and connectors required to allow interconnection between the Everest NET, the motor, the specific feedback or sensors in use and the Master (in case the application is not standalone).

**Heatsink:** when delivering output power, the Everest NET generates small amounts of heat. In low-power applications, the metal case of the Everest NET might be enough to dissipate this heat, but high-power applications or applications running at high ambient temperatures would require to thermally attach the Everest NET to a heatsink.

### 7.1.2. Single-Axis or Multi-Axis approach

The simplest way to integrate Everest NET is to develop an interface board to hold 1 module. This way, 1 Master device can command the Everest NET as a slave, and the Everest NET will control the motor accordingly. The Master can even be part of the interface board, or be externally wired to it.

Multiple Everest NET can also be controlled from a single master along several bus topologies. See Interface and Control section for more information. While the classic approach would be to provide individual interface boards for each Everest NET, and interconnect them by wiring a fieldbus along each node, the compact size and low power dissipation of the Everest NET now allows having a decent number of axis in a single interface board, tracing the fieldbus along the PCB for a maximum performance and minimum wiring complexity.

## 7.2. Schematic Design

Everest NET is designed to be interfaced at **3.3 V levels** (except for specific pins), which would typically be suitable for most modern electronics. However, when interfacing other devices, as sensors, command sources or master controllers, additional adapter electronics might be required to cover a wider range of input voltages. Here, some basic circuits are suggested as a reference design for quick-development of interface boards.

> **About this solution**
> Notice that this solutions are designed to be simple, cost effective, and easy to manufacture. Other solutions from those presented here may also be valid, and even be more suitable for different approaches or design constraints.

**Pinout document required**
See the **Product Description** and the **Pinout** sections for more information on the limits and capabilities of Everest NET.

To start straight, download the project files from the following links. Note that the physical designators in the BOM file will differ from the logical designators shown in this guide.


Bill Of Materials

Schematics

Ingenia recommends to only select RoHS compliant components for designing products which life cycle can easily adhere to WEEE directive.



### 7.2.1. Input Supplies

#### DC Power Supply

Although typically not part of an interface board, but wired outside, this could be one of the main and first elements to take care of, as the way it is dimensioned could affect the rest of the design. Everest NET generates 3-phase currents by means of an inverter topology power stage, so it require a DC power supply to feed its internal DC bus. Selecting the proper voltage, current and power of this supply is typically not as simple as checking the specifications of the target motor. In fact, in most cases the nominal values of the motor will be substantially different from the analogous values of the power supply. To learn more about this, check out the following documents:

- How to dimension a power supply for an Ingenia drive
- Understanding why the motor phase current is different to the power supply currents

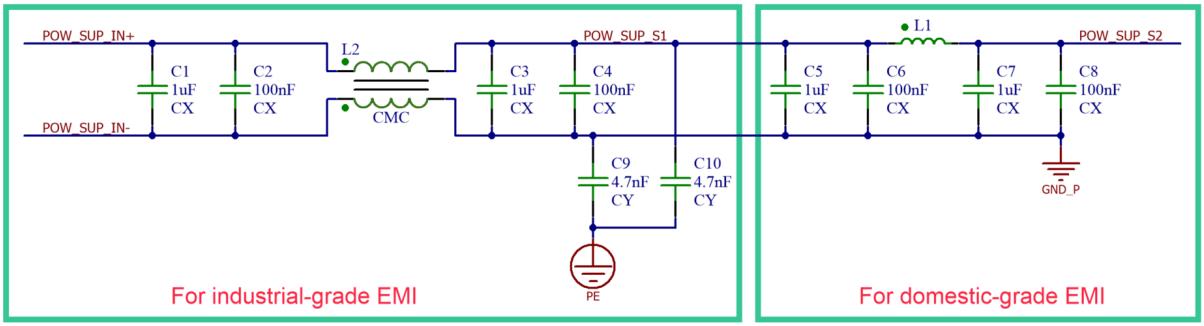
#### DC Bus input stage

Everest NET is a switched power regulator using a very fast state-of-the art switching technology. This allows Everest NET to be extremely efficient, but at the cost of requiring a relatively more sophisticated input stage to avoid transmitting a "sharp" ripple voltage through the power supply lines. This is of an special importance when

sharing the DC bus with other sub-systems or when targeting EMC-related certifications, as CE marking. The most suitable solution will strongly depend on the requirements of the target market or environment (industrial, medical, domestic, automotive...), and the specific dynamics of the load, but in most cases it will consist in 4 elements:

- Input power filter
- Earth decoupling
- DC bus bulk capacitors
- Sourge / ESD protections

The 2 first elements can be resolved by means of a line filter. A 1-stage line filter might be enough in some cases, but in most cases a 2-stage would make it to pass the conducted emissions tests. However, a line filter might be expensive and very bulky compared to the Everest NET, so the on-board discrete solution can be the best trade-off. Here, only very basic and raw indications are given by the following schematic:




The basic protection to fulfill the minimum requirements of most industrial-grade EMC certifications would consist in a power filter targeting the common mode of the DC bus. The input and output capacitors are separated into 1-decade pairs to extend their effectiveness to higher frequencies (this could be done up to 2 decades or even more). The selected values just pretend to be indicative of this. This capacitors should be of X-type ceramic and their voltage must be carefully selected to match the application under a "safety" criteria: keep in mind that **capacity of ceramic capacitors experience a strong derating over voltage**. Decoupling capacitors to Earth C9 and C10 are of crucial importance. They must be of Y-type and rated to safety standards, specially when it comes to have its failure mode guaranteed.

For more demanding EMC requirements, like certifications framed in domestic or automotive standards, an additional filter targeting the differential mode might be required. Here a CLC or Pi filter is suggested, although many others may be valid. This filter is intended to reduce the voltage ripple in the DC bus caused by the fast commutation of the Everest NET, as it propagates through the cables affecting both the conduced and radiated frequency ranges. This is strongly related to the load, as inductance and current ratings of the motor directly affects the DC bus voltage ripple, but DC bus bulk capacity plays a notable role in reducing this effect (see below). In any case, selecting an L1 small enough might be demanding, specially when rated to withstand the current ratings of the Everest NET.

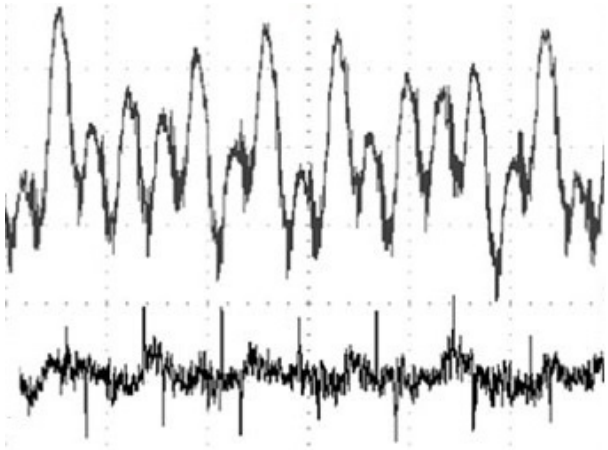
**Contact Ingenia** for further help on this topic.

Second, the **DC bus bulk capacity** plays a crucial role in the EMI response, but also in the motion control. As a dummy rule of thumb, the greater the installed capacity, the better, but at the same time capacitors are big and expensive, so optimising the number and type of the capacitors included in the design is usually something to take care of. Typically, having this capacitors will respond to 3 purposes:

- Reduce voltage ripple in the DC bus to improve EMI ratings
- Reduce voltage ripple in the DC bus to reduce power losses
- Store excess of energy during regenerative braking.

The suggested solution does not target the regenerative braking issue, as an specific circuit is proposed to this purpose below in this guide (see Shunt Braking Resistor Transistor chapter). Then, when it comes to reduce the DC bus voltage ripple, it is interesting to distinguish between 2 phenomena causing it. In the image below this 2 types

of ripple are depicted. The top one has more amplitude, but edges are round and soft, so it mostly carries lower frequency harmonic components. The bottom one has less amplitude, but has sharp edges of a great dV/dt, so it carries higher frequency harmonics. Typically the 2 types of ripple will be seen at the same time over a saw-tooth base shape, but the magnitude of each will typically depend on the amount of current delivered to the motor, and its phase inductance.



High frequency ripple is more likely to increase when the Everest NET is delivering high phase currents. This ripple does not carry much overall energy, but requires capacitors capable of responding at high frequencies with low ESR. Therefore, the best option here will be **ceramic capacitors**, which by nowadays will typically over-perform tantalum, electrolytic or polymer capacitors. Although the minimum required ceramic capacity is already included inside the Everest NET, it is strongly suggested to add at least **30 µF ceramic capacity** externally as close as possible to the Everest NET, to get a reasonable performance in a mid-range application.

Low frequency ripple is more likely to increase when the Everest NET is driving a low inductance motor, specially when driving it at high currents. This ripple can get to carry a lot of energy, and therefore a larger capacity would be required. Here, ceramic capacitors are still the best choice, but installing a large bank of ceramic capacity can be space-consuming and very expensive, while electrolytic capacitors, specially **aluminium electrolytic capacitors**, show much better ratios in capacity per volume at a lower cost. However, be aware that having electrolytic capacitors in a commercial product might entail **serious drawbacks**: they can contain dangerous chemicals, they can explode if mounted in reverse polarity, they could limit the temperature rating of the whole product, and they would probably become the shortest lifetime component of the design (MTBF bottleneck).

**Electrolytic capacitors**
Ingenia recommends not to use electrolytic capacitors unless there is no other way to satisfy the requirements of an application. In such case, select only the highest quality capacitors, with specs such as:

- Temperature rating > 100 ºC
- Low ESR / high ripple withstanding
- Certified lifetime at high temperature (MTBF) > 6000 hours.

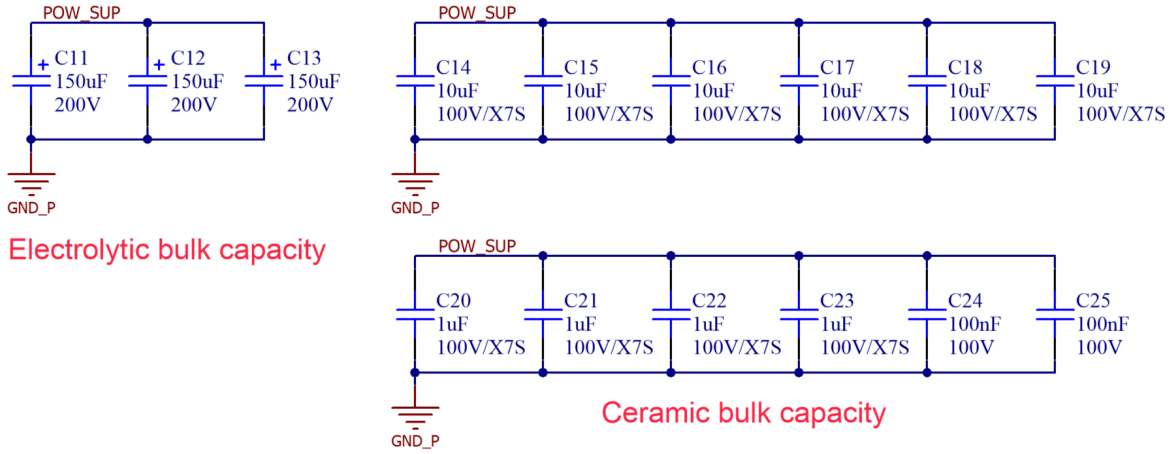
Also, always apply a over-dimension in the voltage rating of electrolytic capacitors of at least x1.3

Finally, it is advisable to include **sourge and ESD protection** in the power DC input to reinforce the immunity ratings of the Everest NET. A TVS could do the job for ESD protection, but might be insufficient in front of a sourge, where suppression of large but very short power peaks is not as relevant as the response in front of a wide and long high-energy peak. To this purpose, varistors are more suitable. As a useful tip, in case a discrete line filter is implemented, it is recommended to place the TVS after the common mode choke: as a CMC acts like an impedance barrier (from the signals propagation point of view) perturbations in the internal DC bus could become fast and short overvoltages when reflected in the CMC. If any of this reflections could reach a dangerous level, the TVS would get rid of it.

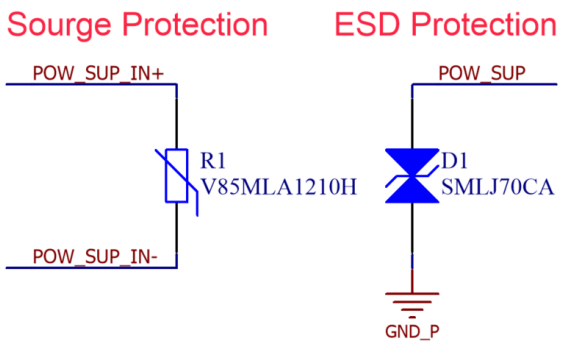
With all this, the following generic solution is proposed:

### Schematic

Ceramic and (optional) electrolytic capacitors:




Sourge and ESD protection:




### Signals description

| Signal | Description |
|---|---|
| POW_SUP_IN+ | Positive terminal of the power supply input |
| POW_SUP_IN- | Negative or reference voltage terminal of the power supply input |
| POW_SUP | Internal DC bus positive supply. Could be connected to Everest NET power pin 1 of P1 if no Inverted Polarity protection is implemented |
| PE | Protective Earth. To be connected to chassis of Everest NET. Could be left unconnected in specific cases |
| GND_P | Internal DC bus reference voltage. To be connected to power pin 2 of P1 in Everest NET |

### Design Notes

- POW_SUP net would be connected to POW_SUP_S1 or POW_SUP_S2 depending on the line filter implemented. If no line filter is on-board, it would be connected to POW_SUP_IN+.
- Select a bidirectional TVS if an Inverse Polarity protection is implemented, and unidirectional TVS otherwise.

- Selected TVS is rated 70 V standoff voltage instead of 80 V. About 1 mA will be sunk through it while the DC bus is supplied to 80 V, but this should not entail a great power loss. On the other hand, by doing this the lower maximum clamping voltage will result in a more effective protection for Everest NET.
- Electrolytic capacity would not be required in most cases.
- Ceramic capacitors should be placed as close to the Everest as possible, being the closest the smallest in capacity.

**Bill of materials**

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| C11, C12, C13 | EKXG201ELL151ML25S | United Chemi-Con | Radial, Ø16x25 mm | Alimimium electrolytic capacitor, 150 µF, 200 V, -40 ºC ~105 ºC, MTBF 1000h @ 105 ºC, 1.89 A @ 100 kHz current ripple |
| C14, C15, C16, C17, C18, C19 | C5750X7S2A106K230KB | TDK | 2220 | Ceramic capacitor, 10 µF, 100 V, X7S |
| C20, C21, C22, C23 | C2012X7S2A105K125AE | TDK | 0805 | Ceramic capacitor, 1 µF, 100 V, X7S |
| C24, C25 | HMK212B7104KG-T | TDK | 0805 | Ceramic capacitor, 100 nF, 100 V, X7R |
| D1 | SMLJ70CA | Bourns | SMC / DO-214-AB | Bidirectional diode TVS, 70 V standoff, 113 V max. clamping, 3000 W |
| R1 | V85MLA1210H | LittlelFuse | 1210 | Varistor, 85 V DC standoff, 250 A max. surge current, 2.5 J max. surge energy |

## Logic supply

Here, it is assumed that a +5 V regulated supply is provided externally. There is a massive bunch of options to select this component, and the best suited will probably be the one fitting the available power source from which to pick the logic supply, whether it is AC or DC. In most cases, the power supply to feed the DC bus will also be the source for the logic supply. In this case a DC/DC will be selected by matching its input voltage range to the maximum expected voltage of the DC bus (including any possible re-injection). This DC/DC could be typically implemented according to 3 approaches: a self-designed discrete DC/DC, an integrated module mounted into the PCB, or a completely external DC/DC wired to the Interface Board. Any solution is valid, whenever the following is met:

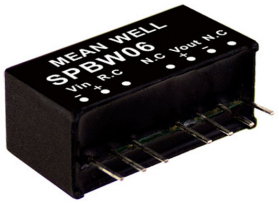
**5 V logic supply DC/DC requirements**

- **Input voltage:** set by application (100 V will cover any possible scenario)
- **Output voltage:** +5 V
- **Output regulation:** ±2% or less
- **Max. ripple:** 200 mVp-p or less
- **Output current:** 800 mA continuous, 1 A continuous preferred.
- **Isolation voltage:** >1.5 kV recommended, although not mandatory in some cases.

Ingenia is committed to a more efficient use of energy and recommends to always select the **highest efficiency** components.

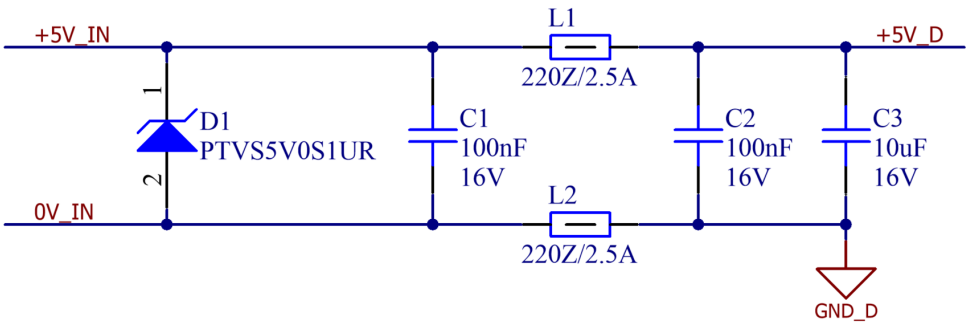
> ⚠ **Output current required**
> The minimum output current specified above is **only for Everest NET**, so does not include the Interface Board self-consumption or its capability to deliver current to other external circuits.

A couple o valid DC/DC examples:

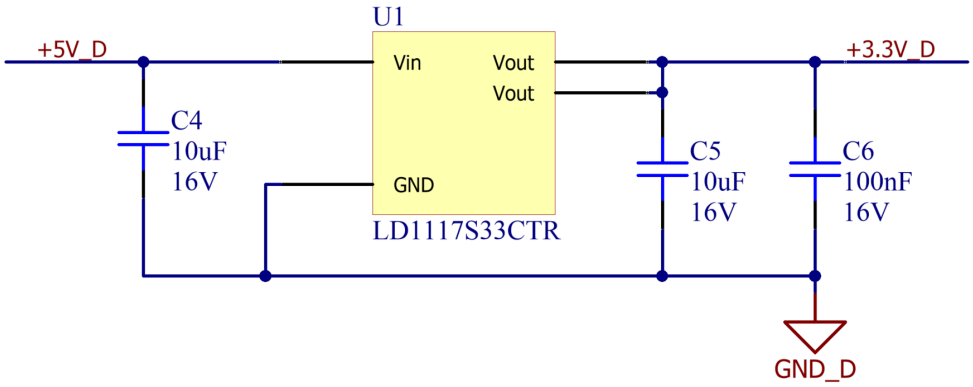
| Image | Part Number | Manufacturer | Type | Description |
|---|---|---|---|---|
|  | RSD-30H-5 | Mean Well | External | 40 V to 160 V input, single 5 V output, 30 W, 4 kV isolation DC/DC |
|   | SPBW06G-05 | Mean Well | PCB | 18 V to 75 V input, single 5 V output, 6 W, 1.5 kW isolation DC/DC |

### Schematic

First, the proposed input stage has a TVS for ESD protection and an input filter. CLC might be good, but here ferrites are used instead instead of inductors for space saving and to focus the attenuation in the highest frequencies.




Second, 5 V is converted to 3.3 V by means of a simple LDO. The Everest NET does not consume any current from this 3.3 V, so it must be enough to cover the self-consumption of the Interface Board plus the amount of current to be sent to external circuits (see 3.3 V and 5 V Output Supplies chapter below).




### Signals description

| Signal | Description |
|---|---|
| +5V_IN | Positive terminal of the 5 V logic supply input |
| 0V_IN | Negative terminal of the 5 V logic supply input |
| +5V_D | +5 V Logic supply to feed both Everest NET and the Interface Board. To be connected to pins 7, 8, 9 and 10 of Everest NET Interface connector |
| +3.3V_D | +3.3 V Logic supply to feed the Interface Board |
| GND_D | Logic supply reference voltage. To be connected to pins 5, 6, 11 and 12 of Everest NET Interface connector |

### Design Notes

- D1 is a unidirectional TVS, meaning that in case of inverse polarity of the 5 V input this will conduce in direct mode. Then, either the power supply voltage will drop once reached the maximum current or the TVS will burn if the power supply is powerful enough. This behaviour is intended, as it works as a very basic inverse polarity protection in addition to its main ESD protection function.
- +5V_D must be connected to pins 7, 8, 9 and 10 of Everest NET Interface connector. All 4 pins must be connected to reach a sufficient current rating from the contacts of the Everest NET Interface connector. Similarly, all 4 pins 5, 6, 11 and 12 should be connected to GND_D.

**3.3 V pins from Everest NET**
Pins 13 and 14 of Everest NET are not supply inputs, so this pins **must not be connected to a supply**. Everest NET is providing this 3.3 V supply outputs to avoid adding external electronics when only simple external circuits are required. However, the maximum current to be drawn from this output is limited to 250 mA, and exceeding it might cause permanent damage to Everest NET, so it is not used in this application example.

### Bill of materials

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| C1, C2, C6 | GRM155R71C104KA88D | Murata | 0402 | Ceramic capacitor, 100 nF, 16 V, X7R |

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| C3, C4, C5 | C2012X7S1C106M125AC | TDK | 0805 | Ceramic capacitor, 10 µF, 16 V, X7S |
| D1 | PTVS5V0S1UR,115 | NXP | SOD-123W | Unidirectional diode TVS, 5 V standoff, 9.2 V max. clamping, 400 W |
| L1, L2 | BLM18SG221TN1D | Murata | 0603 | 2.5 A ferrite bead, 220 Ω @ 100 MHz, 40 mΩ @ DC |
| U1 | LD1117S33CTR | ST Microelectronics | SOT-223-4N | 15 V max. input LDO, fixed 3.3V output, 800 mA |

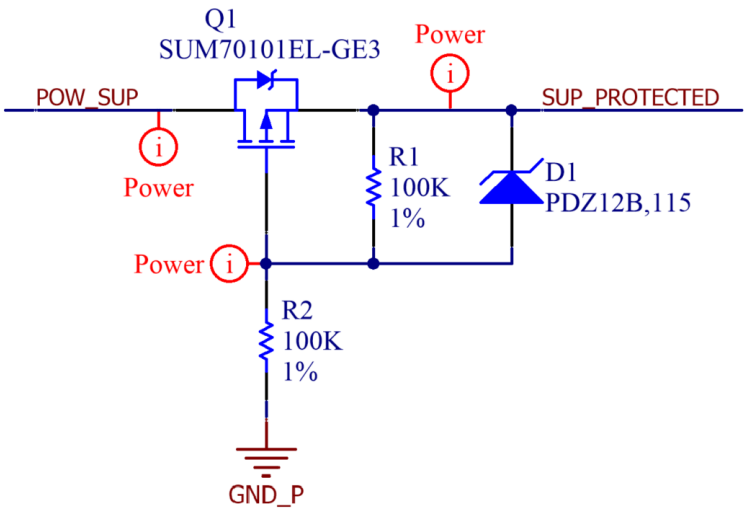
### 7.2.2. Protective circuits

#### Inverse Polarity Protection

This circuit is intended to block any current going into Everest NET when the power supply is connected in inverted polarity. If this circuit is not present, it is suggested to select a polarised power supply connector.

> **Effects of inverted polarity**
> Connecting the power supply under inverted polarity with no protection could cause a massive permanent damage to Everest NET.

**Schematic**




**Signals description**

| Signal | Description |
|---|---|
| POW_SUP | Input from power supply |

| Signal | Description |
|---|---|
| SUP_PROTECTED | Protected power supply. To be connected to power pin 1 of P1 in Everest NET |
| GND_P | Power supply reference voltage. To be connected to power pin 2 of P1 in Everest NET |

**Design Notes**

- In this circuit, the P-channel MOSFET is only polarised properly when the polarity of the supply is correct thanks to resistors R1 and R2. Diode D1 ensures that the maximum gate voltage of the transistor is not exceeded.
- Note that the transistor orientation intentionally allows conduction through the body diode if the supply is polarised properly.

**Bill of materials**

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| D1 | PDZ12B,115 | NXP | SOD-323 | Diode Zener 12 V, 400 mW, 2% tolerance |
| Q1 | SUM70101EL-GE3 | Vishay | TO-263 / $D^2PAK$ | P-channel MOSFET, 100 V, 120 A |
| R1, R2 | RMCF0402FT100K | Stackpole | 0402 | Thick film resistor, 100 kΩ, 1 % tolerance, 1/16 W |

### Shunt Braking Resistor Transistor

During operation the motor normally consumes the energy provided by the drive, but in specific situations this roles change and the motor behaves as a generator. This would happen during short periods of time when the motor is commanded to rapidly decelerate or even change its direction of rotation, or during longer periods of time when the load is driving the motor, like it would happen when a hoist is overloaded. In this cases, although an inverter typically works as a "step-down", it will behave as a "step-up", and could elevate the voltage of the internal DC bus even beyond its maximum ratings, causing permanent damage to the drive and leaving the load completely uncontrolled.

Therefore, this is an over-voltage protection.

To get rid of the problem, 4 strategies are considered. The best one to follow would mostly **depend on the dynamics of the load**, so there is not a best solution to frame all the possible scenarios.

- **Not doing anything:** re-injection could not be an issue, specially when the nominal voltage of the motor is way smaller than the one of the drive (i.e. driving a 24 V motor with Everest NET). If the re-injection is not too strong, the internal DC bus of the drive will increase, but not enough to reach dangerous levels, so the drive will simply withstand it.
- **Using the DC bus capacitors:** if a large bulk capacity is installed close to the Everest NET (not long wires between them) when the DC bus voltage increases because of a re-injection, the capacitors will store the energy, and slowly deliver it afterwards to the motor during normal operation. This method is tremendously ineffective compared to dissipating the excess of energy, but it could do the job in front of short and fast re-injections that would not happen very often, like when the motor sporadically has to change direction of rotation .
- **The system is battery powered:** in this specific case, the re-injection charges the battery. In some applications, like electric vehicles, this might even be an advantage, as it would extend the battery life. However, care must be taken in ensuring that the re-injected current measured in the battery terminals is

not beyond its maximum charging ratings. Also, when the battery is fully charged this method cannot be used.

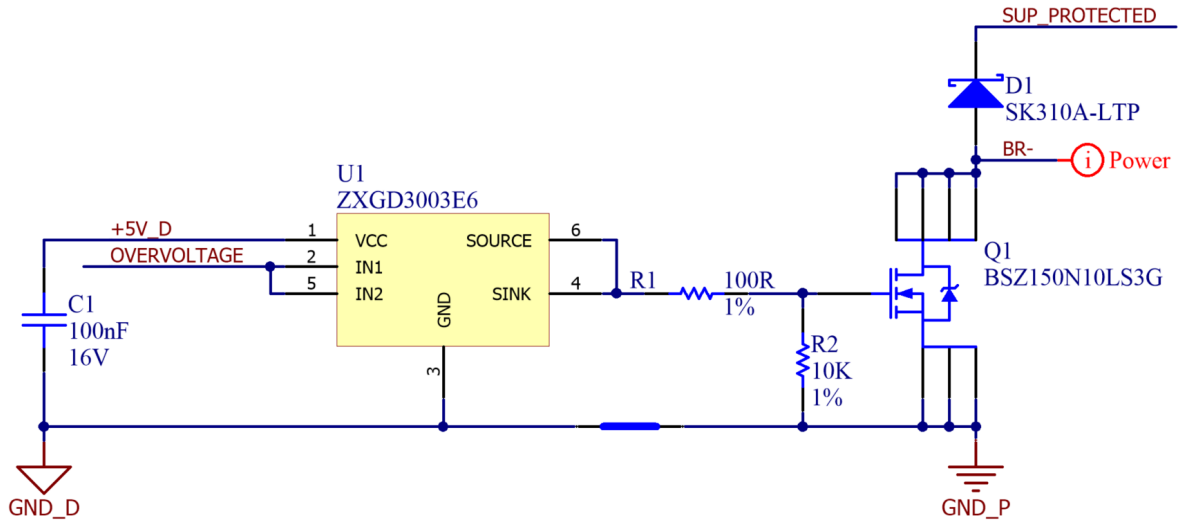
- **Get rid of the excess of energy:** Here a transistor is used to short the DC bus to Ground through a power resistor, which would dissipate the excess of energy as heat. This method has proved to be the most effective (and the less efficient) but has the drawback of requiring a very bulky resistor, which is costly and space-consuming. This method can be implemented with the circuit proposed below.

To learn more about motor re-injection and how to dimension the power resistor, check the following document:

- Dimensioning a Shunt Resistor for Regenerative Braking

> **Multi-axis systems**
> Notice that in multi-axis systems or even when multiple drives share a same DC bus only 1 braking resistor is needed. Even some advanced power supplies have a braking resistor already integrated.

### Schematic




### Signals description

| Signal | Description |
|---|---|
| +5V_D | +5 V Logic supply |
| OVERVOLTAGE | To be connected to any of the GPOx pins of Everest NET Interface connector |
| SUP_PROTECTED | To be connected to power pin 1 of P1 in Everest NET |
| BR- | To be connected to the negative terminal of the power resistor |
| GND_P | Power supply reference voltage. To be connected to power pin 2 of P1 in Everest NET |
| GND_D | Logic supply reference voltage. To be connected to pins 15, 16 or 35 of Everest NET Interface connector |

### Design Notes

- OVERVOLTAGE net must be tied to any of the GPOx pins of Everest NET Interface connector (pins 17, 29, 30 or 31). Then, **the Everest NET must be configured** to map the Overvoltage signalling functionality to this

specific GPO, which will then stop working as a general purpose digital output. Check out the **Summit Series Reference Manual** to know how to configure this feature.
- Connect this protection as close to the Everest NET as possible. If an Inverse Polarity Protection is also implemented, connect their SUP_PROTECTED nets together.
- The positive terminal of the power resistor could be connected to SUP_PROTECTED net or externally to the positive terminal of the power supply.
- The net-tie between the GND_D and the GND_P allows sharing the same reference voltage while controlling the return path in the layout phase.
- C1 is a decoupling capacitor for U1.
- 3.3 V could be enough to excite the gate of Q1, although at least 4.5 V is recommended to reduce power losses. In any case, it is not recommended to drive Q1 directly from a GPOx pin of Everest NET.
- The wheeling diode D1 provides a discharge path for the energy stored in the power resistor (specially for wirewound type of resistor).

**Commutation requirements**
Once a power resistor is properly selected, meaning that it fits the dynamics of the load during re-injection, there is no need to modulate the excitation of Q1. Not only no PWM is required, but it would even have a negative effect by increasing the power losses in the transistor with no need. Still, the transistor will switch at a frequency within the scale of 10 Hz to 1 kHz, depending on the over-voltage detection hysteresis configured in the Everest NET.

**Bill of materials**

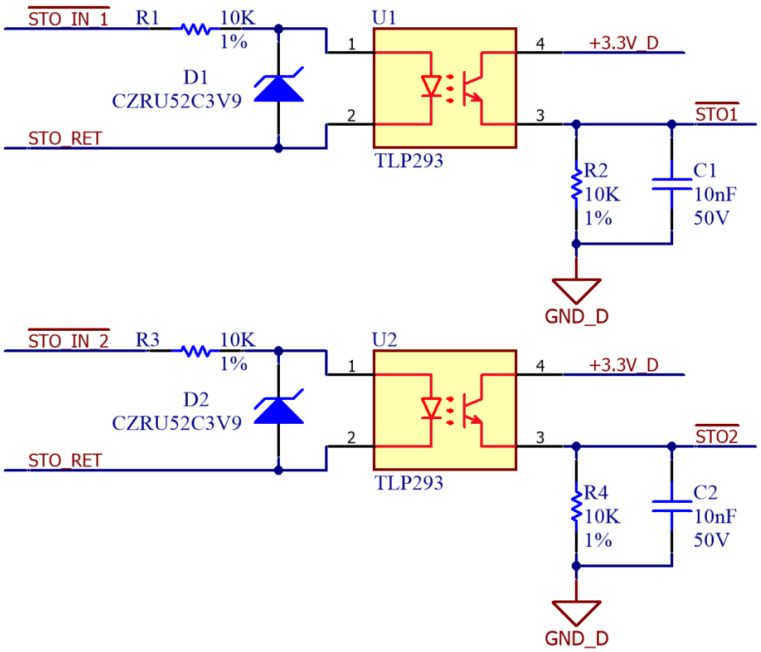
| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| C1 | GRM155R71C104KA88D | Murata | 0402 | Ceramic capacitor, 100 nF, 16 V, X7R |
| D1 | SK310A-LTP | Micro Commercial | SMA / DO-214AC | Diode Schottky, 3 A, 100 V |
| Q1 | BSZ150N10LS3 G | Infineon | TSDSON-8 | Logic-level N-Channel MOSFET, 100 V, 40 A |
| R1 | RMCF0402FT100R | Stackpole | 0402 | Thick film resistor, 100 Ω, 1 % tolerance, 1/16 W |
| R2 | RMCF0402FT10K0 | Stackpole | 0402 | Thick film resistor, 10 kΩ, 1 % tolerance, 1/16 W |
| U1 | ZXGD3003E6TA | Diodes Incorporated | SOT-23-6 | Low-side gate driver, 40 V, 5 A peak |

### Safe Torque Off (STO)

This circuit provides a dual, protected and isolated input interface for the Torque Off functionality built-in the Everest NET. Whenever any of the input signals carry a low level, the power stage of the Everest NET will remain unable to generate a rotating magnetic field inside the motor, which means it will be unable to generate torque. The high level is up to 30 V tolerant.

**Care for certification**
Note that this circuit may not be compliant with major safety on machinery standards (like IEC 61800 or others). To get support on targeting this king of certification, please contact Ingenia.

### Schematic




### Signals description

| Signal | Description |
|---|---|
| +3.3V_D | +3.3V Logic supply |
| \STO_IN_1 | Safe Torque Off inputs positive terminal |
| \STO_IN_2 | |
| STO_RET | Safe Torque Off inputs negative or reference terminal |
| \STO1 | To be connected to pin 33 of Everest NET Interface connector |
| \STO2 | To be connected to pin 34 of Everest NET Interface connector |
| GND_D | Logic supply reference voltage. To be connected to pin 35 of Everest NET Interface connector |

### Design Notes

- STO_RET is tied together from the 2 circuits, but could be wired separately.
- Zener diodes D1 and D2 provide 2 protective functionalities at the same time. First, they protect against overvoltage of the optocopupler's emitter by saturating voltage thanks to the current limited by resistors R1 and R3. This also expands the operating range of the input to 24 V levels (30 V maximum). Second, they protect against inverted polarity of the input voltage, as in this case they will conduct current in the forward direction, and still the current will be limited by resistors R1 and R3.

**Not using STO**
When not requiring STO inputs, signals **\STO1 and \STO2 must be tied to a high level**. +3.3 V or +5 V can be used. **Do not use a series or pull-up resistor, tie them directly**.

**Bill of materials**

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| C1, C2 | C0402C103K5RACTU | Kemet | 0402 | Ceramic capacitor, 10 nF, 50 V, X7R |
| D1, D2 | CZRU52C3V9 | Comchip | 0603 | Diode Zener 150 mW 5% 0603. 3.9 V @ 5mA, 3.3 V @ 1mA |
| R1, R3 | ERJ-P06F1002V | Panasonic | 0805 | Resistor, 0805, 10kohm, 1/2 W, pulse withstanding |
| R2, R4 | RMCF0402FT10K0 | Stackpole | 0402 | Thick film resistor, 10 kΩ, 1 % tolerance, 1/16 W |
| U1, U2 | TLP293(BL-TPL,E | Toshiba | 4-SOIC | Transistor output optocoupler, 3750 Vrms isolation, 50% min. CTR |

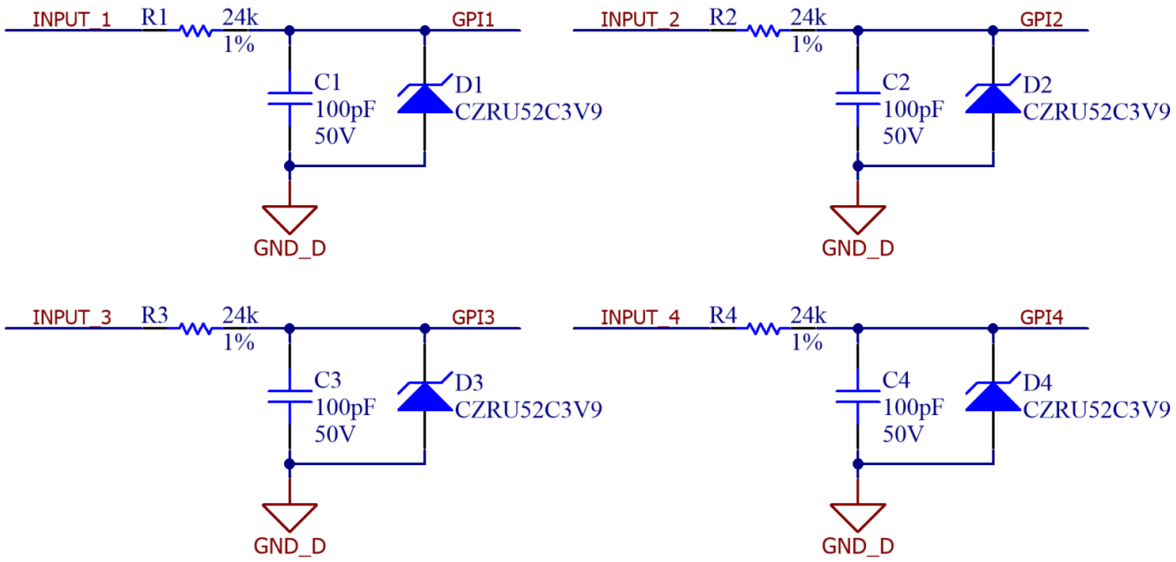
### 7.2.3. Inputs and Outputs

#### Digital Inputs

Simple solution to adapt a rather wide range of input voltages to 3.3 V levels.

**Schematic**

A resistor limits the current while a Zener diode saturates the voltage. Everest NET will detect as "low" any voltage lower than 0.8, and as "high" any voltage greater than 3 V, while still being tolerant to input voltages up to 30 V.



**Signals description**

| Signal | Description |
|---|---|
| INPUT_1 | Digital inputs 1 to 4 |
| INPUT_2 | |
| INPUT_3 | |
| INPUT_4 | |
| GPI1 | To be connected to pin 18 of Everest NET Interface connector |
| GPI2 | To be connected to pin 19 of Everest NET Interface connector |
| GPI3 | To be connected to pin 20 of Everest NET Interface connector |
| GPI4 | To be connected to pin 32 of Everest NET Interface connector |
| GND_D | Logic supply reference voltage. To be connected to pins 15, 16 or 35 of Everest NET Interface connector |

**Design Notes**

- For simplicity, the proposed solution is not opto-isolated. Therefore, the input signals generator (could be a PLC or other controller) must share the Ground with Everest NET.
- 24 kΩ is not a random value. It is intended to fit the voltage-current characteristic curve of the Zener diodes.
- Capacitors form a 1st order filter with the resistors. This will typically reject high-frequency noise coupled to the wiring in most of the cases.

**Bill of materials**

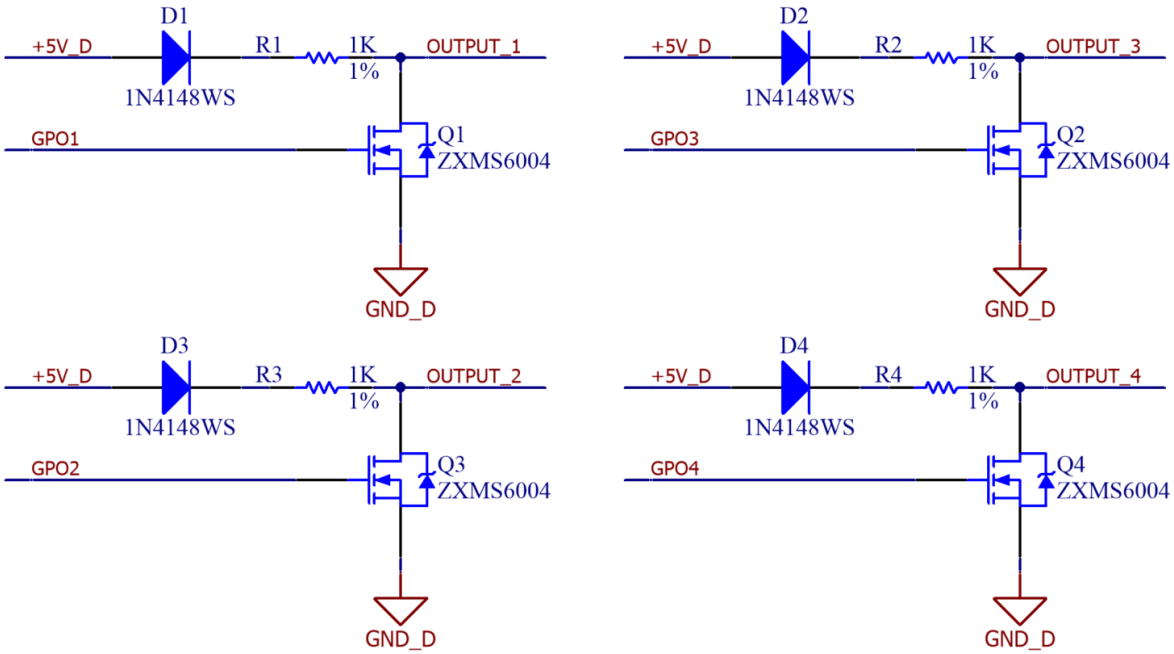
| | | | | |
|---|---|---|---|---|
| R1, R2, R3, R4 | RC0603FR-0724KL | Yageo | 0603 | Thick film resistor, 24 kΩ, 1 % tolerance, 0.1 W |
| C1, C2, C3, C4 | CC0402JRNPO9BN101 | Yageo | 0402 | Ceramic capacitor, 100 pF, 50 V, NP0 |
| D1, D2, D3, D4 | CZRU52C3V9 | Comchip | 0603 | Diode Zener 150 mW 5% 0603. 3.9 V @ 5mA, 3.3 V @ 1mA |
| **Designator** | **Part Number** | **Manufacturer** | **Package** | **Value / Description** |

## Digital Outputs

This simple circuit can be used to convert the 3.3 V push-pull digital outputs of Everest NET into 5 V open collector with weak pull-ups. This will invert the logic polarity of the output, but at the same time it will provide the capability of driving greater loads.

**Schematic**

The following circuits should allow driving loads up to 48 V and 1 A safely.




**Signals description**

| Signal | Description |
|---|---|
| +5V_D | +5 V Logic supply |
| OUTPUT_1 | Digital outputs 1 to 4 |
| OUTPUT_2 | |
| OUTPUT_3 | |
| OUTPUT_4 | |
| GPO1 | To be connected to pin 29 of Everest NET Interface connector |
| GPO2 | To be connected to pin 30 of Everest NET Interface connector |
| GPO3 | To be connected to pin 31 of Everest NET Interface connector |
| GPO4 | To be connected to pin 17 of Everest NET Interface connector |
| GND_D | Logic supply reference voltage. To be connected to pins 15, 16 or 35 of Everest NET Interface connector |

**Design Notes**

- The suggested MOSFETs do not require gate biasing.
- Also, the suggested MOSFETs feature short-circuit, overload, over-temperature and inverse polarity protection.
- This solution should allow driving small inductive loads with no need of a wheeling diode.

- When driving loads in open collector configuration, only the negative terminal of the load must be connected to the output. Although it is an output, it will work by sinking current. The positive terminal of the load would be connected to a power source which Ground terminal is shared with Everest NET.
- When using the load in push-pull configuration, the 1 kΩ resistor set the output impedance and limit the current. In this case, note that the polarity of the GPOx signal coming from Everest NET will be inverted in the output.

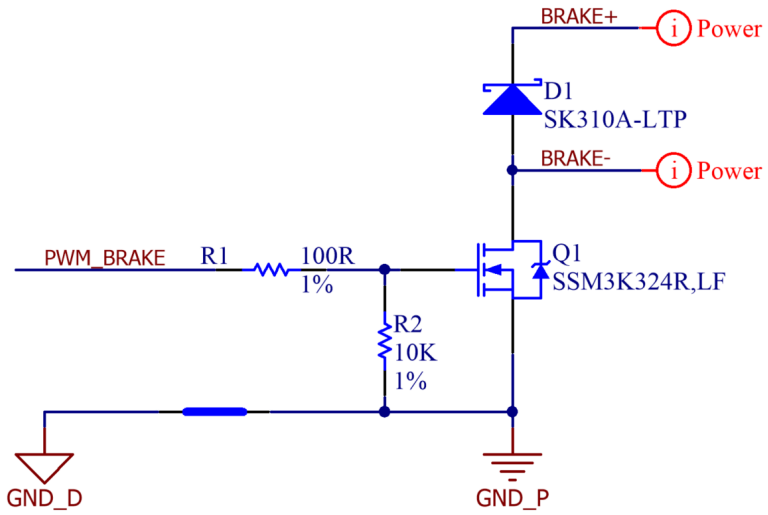
**Bill of materials**

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| D1, D2, D3, D4 | 1N4148WS | Fairchild | SOD-323F | Diode rectifier 75 V, 150 mA |
| R1, R2, R3, R4 | RMCF0402FT1K00 | Stackpole | 0402 | Thick film resistor, 1 kΩ, 1 % tolerance, 1/16 W |
| Q1, Q2, Q3, Q4 | ZXMS6004FFTA | Diodes Inc. | SOT-23F | N-channel MOSFET , 60 V, 1.3 A |

## Mechanical Brake Output

Because of its similarities, the same circuit as the one proposed in the Shunt Braking Resistor Transistor section could be used. However, for cost and space optimisation, the following circuit is proposed. This would provide a 24 V tolerant open collector output for driving a mechanical brake of the solenoid type.

**Schematic**




**Signals description**

| Signal | Description |
|---|---|
| BAKE+ | Positive terminal of the brake solenoid |
| BAKE- | Negative terminal of the brake solenoid |
| PWM_BRAKE | To be connected to pin 41 of Everest NET Interface connector |

| Signal | Description |
|---|---|
| GND_D | Logic supply reference voltage. To be connected to pins 38 or 46 of Everest NET Interface connector |
| GND_P | Power supply reference voltage. To be connected to power pin 2 of P1 in Everest NET |

**Design Notes**

- Signal BRAKE+ is to be connected to the positive terminal of the brake solenoid, and at the same time to the positive terminal of the brake power supply. The negative terminal of the brake power supply must be tied to GND_P.
- If the DC bus is supplied at 24 V or less, the signal BRAKE+ could be tied to SUP_PROTECTED or externally connected to the positive terminal of the power supply.
- The net-tie between the GND_D and the GND_P allows sharing the same reference voltage while controlling the return path in the layout phase.
- As a solenoid is a highly inductive load, the wheeling diode D1 provides a discharge path for the energy stored in it.

⚠ **In case of a low voltage DC bus**
Everest NET DC bus can be driven from a very low voltage power supply, but still a 24 V brake might be required. In the event that the **DC bus is lower than the brake driving voltage, the signal BRAKE+ must not be tied to the DC bus** (either SUP_PROTECTED, POW_SUP or power pin 1 of P1 in Everest NET). If doing so, diode D1 would short the DC bus to a greater voltage, allowing a great current through it, and most probably burning it.

**Bill of materials**

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| D1 | SK310A-LTP | Micro Commercial | SMA / DO-214AC | Diode Schottky, 3 A, 100 V |
| Q1 | SSM3K324R,LF | Toshiba | SOT-23-3N | Logic-level N-Channel MOSFET, 30 V, 4 A |
| R1 | RMCF0402FT100R | Stackpole | 0402 | Thick film resistor, 100 Ω, 1 % tolerance, 1/16 W |
| R2 | RMCF0402FT10K0 | Stackpole | 0402 | Thick film resistor, 10 kΩ, 1 % tolerance, 1/16 W |

### 7.2.4. Output Supplies

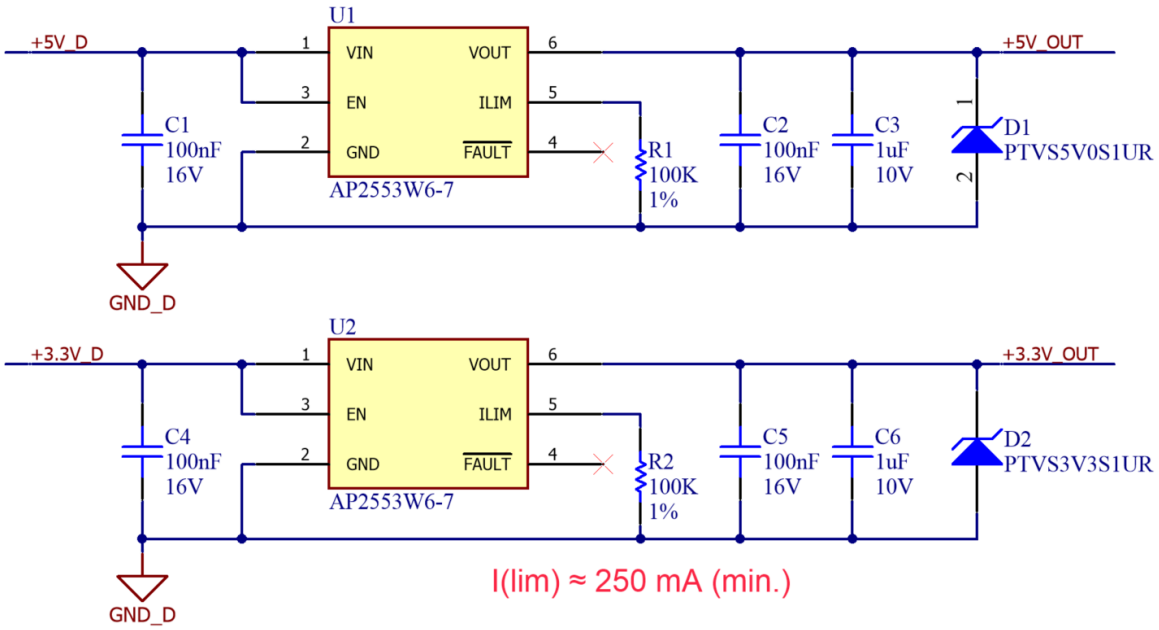
#### 3.3 V and 5 V Output Supplies

To be able of supplying external circuitry, like feedback sensors or command sources, two load switches are implemented as identical circuits. This would limit the current drawn from the outside, providing both short-circuit and overload protection, and thus maintaining the internal logic supply lines safe. Additionally, TVS diodes are added for ESD protection.

**External current consumption**
Both 5 V and 3.3 V internal logic supplies must be able of handling the self-consumption plus the maximum current limit set here. Otherwise the internal logic supplies could drop before the load switch overcurrent protection acts, which could cause failures of diverse nature. See Logic supply chapter above for more information.

**GND connection required**
External circuitry supplied this way must have its reference or Ground voltage connected to GND_D

### Schematic




### Signals description

| Signal | Description |
|---|---|
| +5V_D | +5 V internal Logic supply |
| +3.3V_D | +3.3 V internal Logic supply |
| +5V_OUT | +5 V output supply for external circuits |
| +3.3V_OUT | +3.3 V output supply for external circuits |
| GND_D | To be connected to GND_D in the Everest NET Interface connector |

### Design Notes

- R1 and R2 set the current limit. Considering the tolerances of both the load switch and the resistor, the current would be limited to a minimum of 246 mA and a maximum of 315 mA, with a typical value of 282 mA. Thermal drifts are not considered in this calculation.

- This approach provides a quite rugged overcurrent protection, but it is very weak in front of overvoltage. Any voltage over 6.5 V in the output might cause permanent damage to the load switch. TVS will help here, put not to become an overvoltage protection in DC.

**Bill of materials**

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| C1, C2, C4, C5 | GRM155R71C104KA88D | Murata | 0402 | Ceramic capacitor, 100 nF, 16 V, X7R |
| C3, C6 | C1005X7S1A105K050BC | TDK | 0402 | Ceramic capacitor, 1 µF, 10 V, X7S |
| D1 | PTVS5V0S1UR,115 | NXP | SOD-123W | Unidirectional diode TVS, 5 V standoff, 9.2 V max. clamping, 400 W |
| D2 | PTVS3V3S1UR,115 | NXP | SOD-123W | Unidirectional diode TVS, 3.3 V standoff, 8 V max. clamping, 400 W |
| R1, R2 | RMCF0402FT100K | Stackpole | 0402 | Thick film resistor, 100 kΩ, 1 % tolerance, 1/16 W |
| U1, U2 | AP2553W6-7 | Diodes Incorporated | SOT-23-6N | 5.5 V self-protected load switch, adjustable current limit |

### 7.2.5. Communications

Everest NET is compatible with EtherCAT and CANopen communication protocols. An Ethernet physical layer will be required to interface the Everest NET through EtherCAT, while a CAN physical layer will do for CANopen. Although the Everest NET hardware is the same, each protocol is enabled by a **different firmware**, which can be freely downloaded and installed from the configuration software (see **Interface and Control** section).

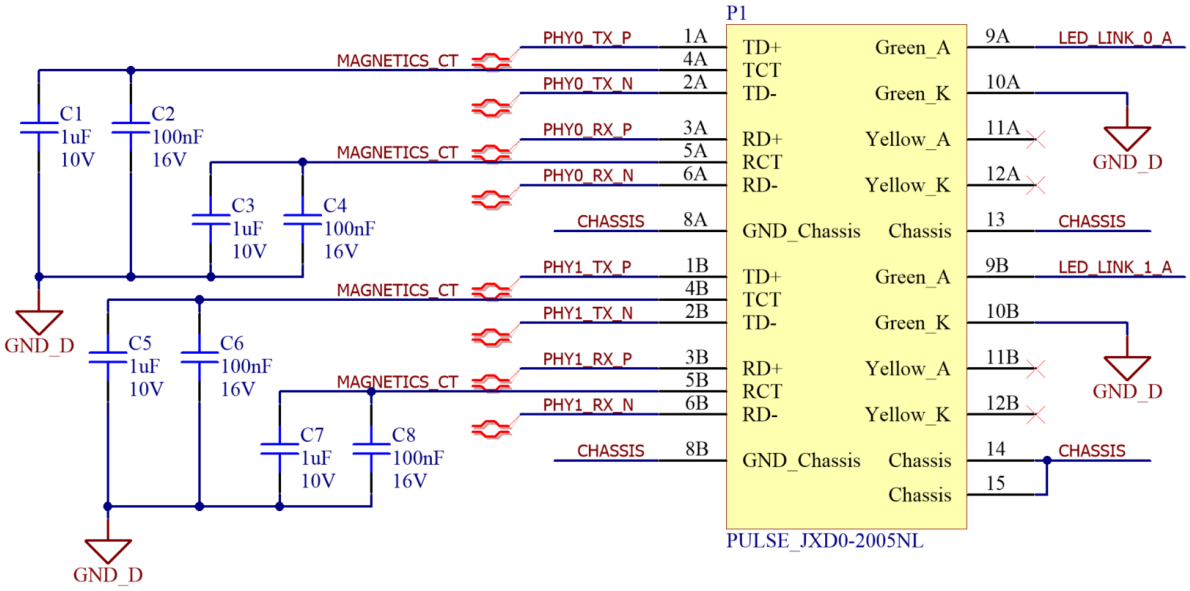
Therefore, from the 2 circuits proposed below, typically just one would be implemented.

#### Ethernet (physical layer for EtherCAT)

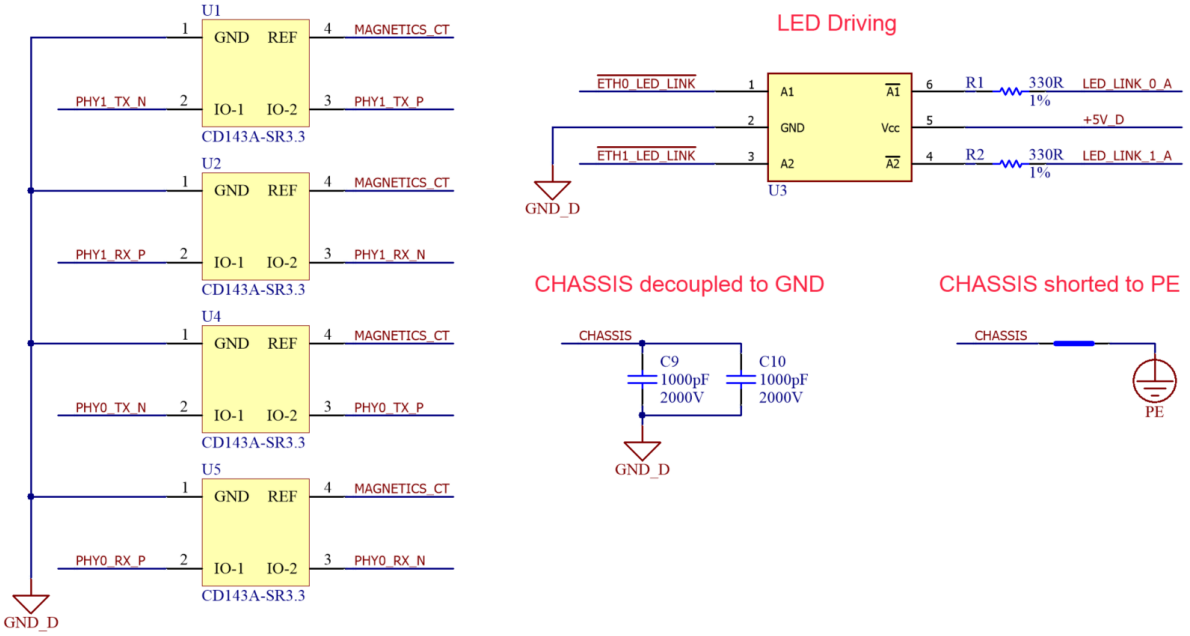
This circuit includes the required electronics and protections required to set an Ethernet physical layer according to 100BASE-T standards.

**Schematic**

The main component is a dual RJ-45 connector with included magnetics. Decouplings and terminations to transformers center tap is included inside its housing.




Additionally, specialised TVS provide protection in front of an ESD or surge event, the chassis of the RJ-45 connector (shorted to PE) is decouped to GND for safety and LEDs also integrated in the RJ-45 housing are driven from Everest NET.




**Link LED signals**
Never drive an LED directly from \ETH0_LED_LINK or \ETH1_LED_LINK signals. Always use an inverting buffer. See Design Notes below.

### Signals description

| Signal | Description |
|---|---|
| +5V_D | +5 V Logic supply |

| Signal | Description |
|---|---|
| MAGNETICS_CT | Center tap voltage of magnetics. To be connected to pin 13 of Everest NET Interface connector. |
| PHY0_TX_P | EtherCAT differential pairs. To be connected to pins 71 to 78 of Everest NET Interface connector |
| PHY0_TX_N | |
| PHY0_RX_P | |
| PHY0_RX_N | |
| PHY1_TX_P | |
| PHY1_TX_N | |
| PHY1_RX_P | |
| PHY1_RX_N | |
| \ETH0_LED_LINK | Ethernet Port 0 Link LED signalling. Must be buffered and inverted to drive a LED |
| LED_LINK_0_A | Anode of green LED integrated in Port 0 of the RJ-45 connector |
| \ETH1_LED_LINK | Ethernet Port 0 Link LED signalling. Must be buffered and inverted to drive a LED |
| LED_LINK_1_A | Anode of green LED integrated in Port 1 of the RJ-45 connector |
| CHASSIS | Metallic case of the RJ-45 connector |
| PE | Protective Earth |
| GND_D | Logic supply reference voltage. To be connected to pins 69, 70, 79 and 80 of Everest NET Interface connector |

**Design Notes**

- Center tap voltage must be managed by Everest NET. Therefore, it **must be connected to pin 13 of Interface connector only**, not to pin 14 and not to any other voltage source or load.
- Signals \ETH0_LED_LINK and \ETH1_LED_LINK behave as configuration inputs during boot up of Everest NET. Therefore, **this signals must always be connected to a high impedance**, which means they should never drive an LED directly, but by means of an inverting buffer (U3). If this advice is not respected, the Ethernet physical layer could not work at all.
- LEDs could be driven from +3.3 V instead of +5 V to simplify logic supply. However this would entail a way less stable control of the LEDs brightness.
- Although TVS do not affect the basic functionality of the Ethernet physical layer, it is not recommended to remove this protection, as it is mandatory to comply with the standard.
- CHASSIS may not be connected to PE (Protective Earth), as the best way to connect the CHASSIS highly depends on the electrical scenario the system will be working into.

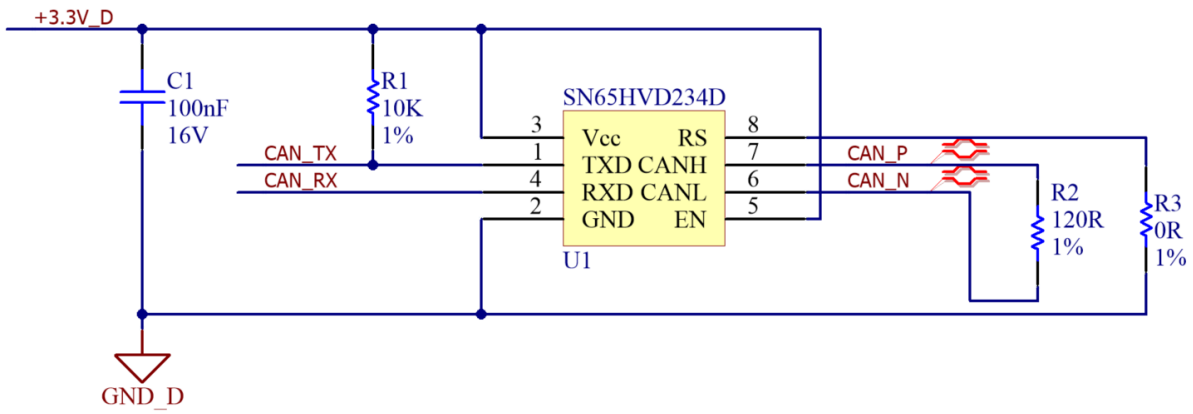
**Bill of materials**

| | | | | |
|---|---|---|---|---|
| C1, C3, C5, C7 | C1005X7S1A105K050BC | TDK | 0402 | Ceramic capacitor, 1 µF, 10 V, X7S |
| C2, C4, C6, C8 | GRM155R71C104KA88D | Murata | 0402 | Ceramic capacitor, 100 nF, 16 V, X7R |
| C9, C10 | 1206GC102KAT1A | AVX | 1206 | Ceramic capacitor, 1 nF, 2000 V, X7R |
| P1 | JXD0-2005NL | Pulse | RJ45 8p8c | Dual RJ45 connector with magnetics, shielded, yellow and green LEDs included |
| R1, R2 | RMCF0603FT330R | Stackpole | 0603 | Thick film resistor, 330 Ω, 1 % tolerance, 0.1 W |
| U1, U2, U4, U5 | CD143A-SR3.3 | Bourns | SOT143 | Steering / TVS diode array, 3.3 V standoff, Ethernet application-specific |
| U3 | NL27WZ14DFT2G | ON Semiconductor | SC88 / SC70-6 | Dual Schmitt trigger inverting buffer, 24 mA output, 1.65 V to 5.5 V supply |
| **Designator** | **Part Number** | **Manufacturer** | **Package** | **Value / Description** |

## CAN (physical layer for CANopen)

This transceiver will convert the differential levels of the CAN bus physical layer into 3.3 V levels.

**Schematic**




**Signals description**

| Signal | Description |
|---|---|
| +3.3V_D | +3.3 V Logic supply |
| CAN_P | Positive terminal of CAN bus (CAN High) |

| Signal | Description |
|---|---|
| CAN_N | Negative terminal of CAN bus (CAN Low) |
| CAN_RX | To be connected to pin 55 of Everest NET Interface connector |
| CAN_TX | To be connected to pin 57 of Everest NET Interface connector |
| GND_D | Logic supply reference voltage. To be connected to pin 59 of Everest NET Interface connector |

**Design Notes**

- The design includes a **termination resistor** (R2), but this shall be included only in the first and last node of the bus (including the Master).
- Resistor R3 is used to limit the slope rate of the signal transition, which can have a significant impact in terms of EMC. If this becomes an issue, a value of 10 kΩ can entail a big reduction of EMI, while still being able to communicate at 1 Mbps.
- Resistor R1 is required by Everest NET during boot-up self-configuration.
- C1 is a decoupling capacitor for U1.

**Bill of materials**

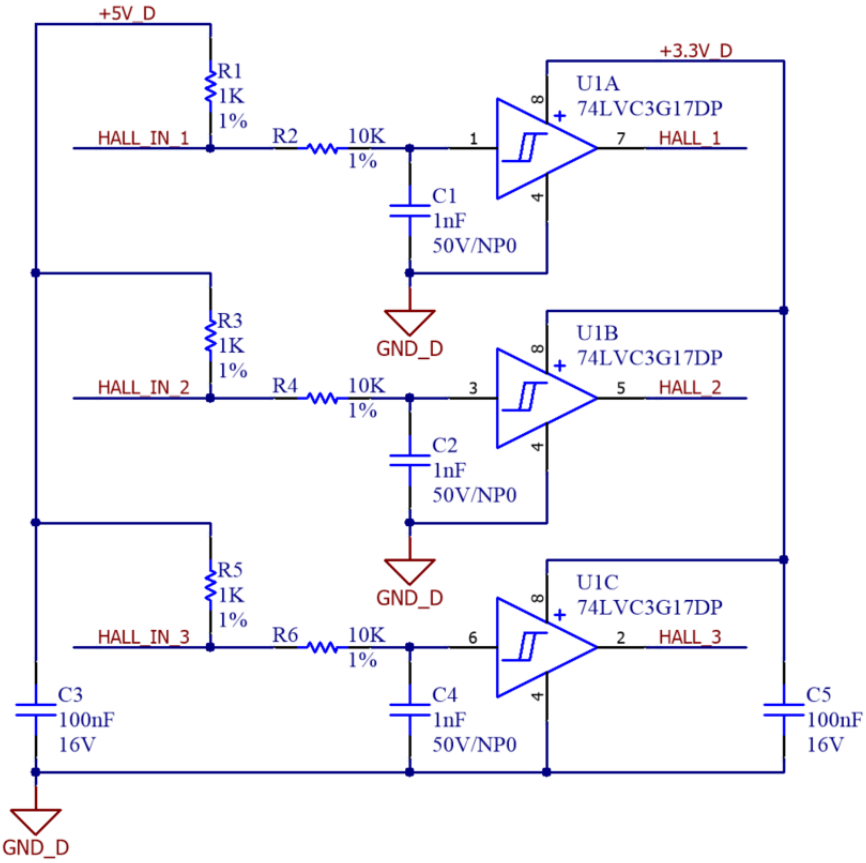
| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| C1 | GRM155R71C104KA88D | Murata | 0402 | Ceramic capacitor, 100 nF, 16 V, X7R |
| R1 | RMCF0402FT10K0 | Stackpole | 0402 | Thick film resistor, 10 kΩ, 1 % tolerance, 1/16 W |
| R2 | MCHP05W4F1200T5E | Multicomp | 0805 | Thick film resistor, 120 Ω, 1 % tolerance, 1/4 W |
| R3 | MC00625W040210R | Multicomp | 0402 | Thick film resistor, 0 Ω jumper, 1/16 W |
| U1 | SN65HVD234DR | Texas Instruments | 8-SOIC | CAN transceiver, 1 Mbps |

### 7.2.6. Feedbacks

#### Digital Halls

This circuit assume a typical open collector output from a digital hall circuitry and provides 5 V level pull-ups to interface it. Then, a 1st order RC filter plus an Schmitt trigger buffer filter the signal and translates it to 3.3 V levels for a decent ruggedness against noise.

### Schematic




### Signals description

| Signal | Description |
|---|---|
| +3.3V_D | +3.3 V Logic supply |
| +5V_D | +5 V Logic supply |
| HALL_IN_1 | Digital hall inputs from motor |
| HALL_IN_2 | |
| HALL_IN_3 | |
| HALL_1 | To be connected to pins 17, 19 and 21 of Everest NET Feedback connector |
| HALL_1 | |
| HALL_1 | |
| GND_D | Logic supply reference voltage. To be connected to pin 15 of Everest NET Feedback connector |

### Design Notes

- U1 is represented as 3 symbols, A, B and C, but still a single component.

- The RC filter makes a 1st order $f_c$(-3dB) ≈ 16 kHz, but having the bandwidth of U1, the circuit should work fine with signals up to 5 kHz.
- C5 is decoupling capacitor for U1.
- U1 alone might have sufficient ESD protection.

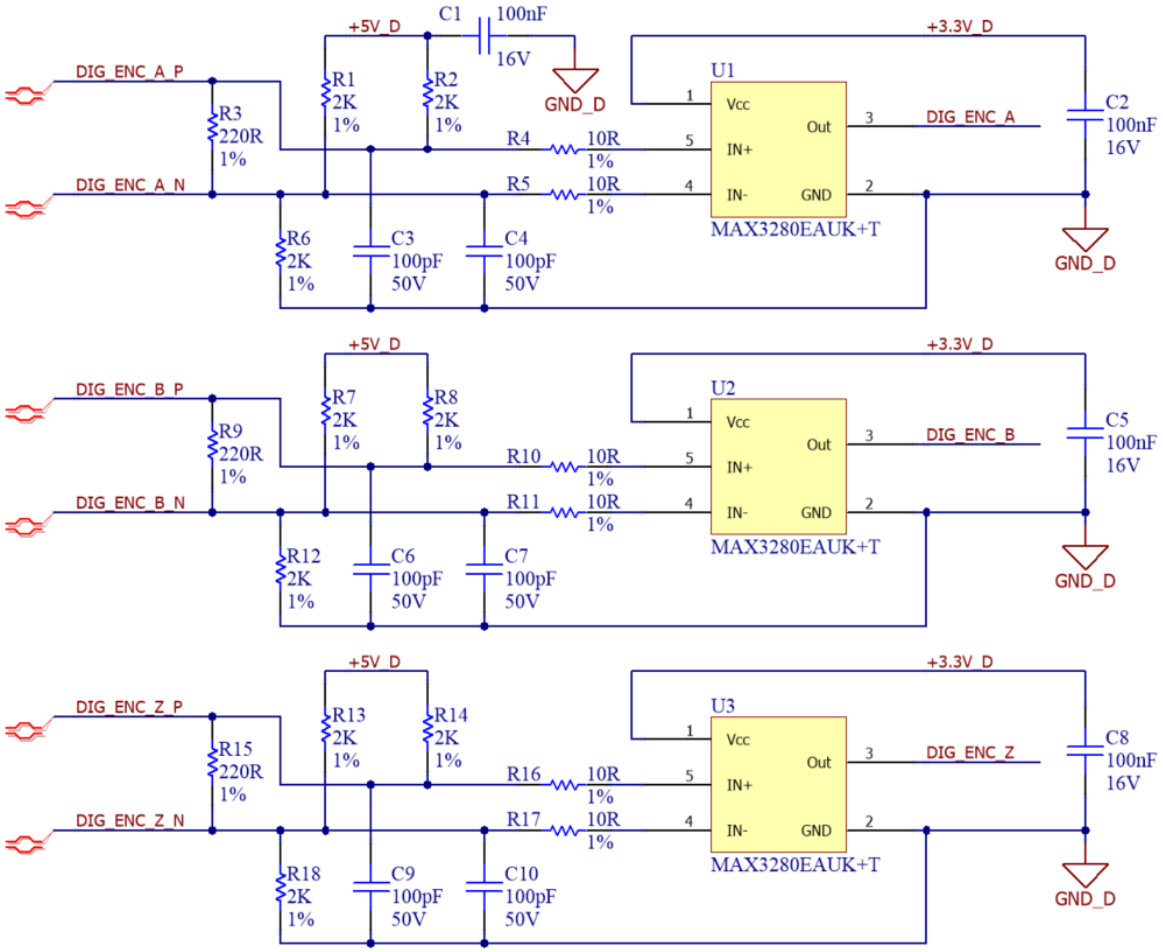
**Bill of materials**

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| C1, C2, C4 | C1005NP01H102J050BA | TDK | 0402 | Ceramic capacitor, 1 nF, 50 V, NP0 |
| C3, C5 | GRM155R71C104KA88D | Murata | 0402 | Ceramic capacitor, 100 nF, 16 V, X7R |
| R1, R3, R5 | RMCF0402FT1K00 | Stackpole | 0402 | Thick film resistor, 1 kΩ, 1 % tolerance, 1/16 W |
| R2, R4, R6 | RMCF0402FT10K0 | Stackpole | 0402 | Thick film resistor, 10 kΩ, 1 % tolerance, 1/16 W |
| U1 | 74LVC3G17DP,125 | NXP | 8-TSSOP | Non-inverting triple Schmitt trigger buffer, 24 mA output, 1.65 V to 5.5 V supply |

### Quadrature / Incremental Encoder

This circuit RS422/RS485 line receivers as hysteresis comparators. Line receivers perform very good in this kind of circuits due to its its price, high speed response, common mode tolerance and built-in ESD protection. The negative terminal is biased to 2.5 V for compatibility with single-ended encoders, while the positive terminal is pulled-up for an extra robustness in front of a weak and noisy connection.

### Schematic




### Signals description

| Signal | Description |
|---|---|
| +3.3V_D | +3.3 V Logic supply |
| +5V_D | +5 V Logic supply |
| DIG_ENC_A | To be connected to pins 24, 26 and 28 of Everest NET Feedback connector to feed Digital Encoder 1 |
| DIG_ENC_B | |
| DIG_ENC_Z | To be connected to pins 30, 32 and 34 of Everest NET Feedback connector to feed Digital Encoder 2 |
| DIG_ENC_A_P | Incremental encoder channel A differential pair |
| DIG_ENC_A_N | |
| DIG_ENC_B_P | Incremental encoder channel B differential pair |
| DIG_ENC_B_N | |

| Signal | Description |
|---|---|
| DIG_ENC_Z_P | Incremental encoder Index differential pair |
| DIG_ENC_Z_N | |
| GND_D | Logic supply reference voltage. To be connected to pin 22 of Everest NET Feedback connector whenever Digital Encoder 1 is wired. Connect to pin 36 of Everest NET Feedback connector if Digital Encoder 2 is wired |

**Design Notes**

- Resistors R3, R9 and R15 are termination resistors. 120 Ω could also be used in case of a harsh electromagnetic environment.
- C3, C4, C6, C7, C9 and C10, in combination with R4, R5, R10, R11, R16 and R17, perform a protective function of the transceiver in front of spikes or ESD, and at the same time increases immunity to common mode noise. Capacitors could be increased up to 220 pF to reinforce this effects even more if required.
- C2, C5 and C8 are decoupling capacitors for U1, U2 and U3.
- To interface a single-ended encoder, connect the ABZ signals to the positive terminal of each differential pair and leave the negative unconnected. It is mandatory that the encoder and the Everest NET then share their reference voltage or Ground.

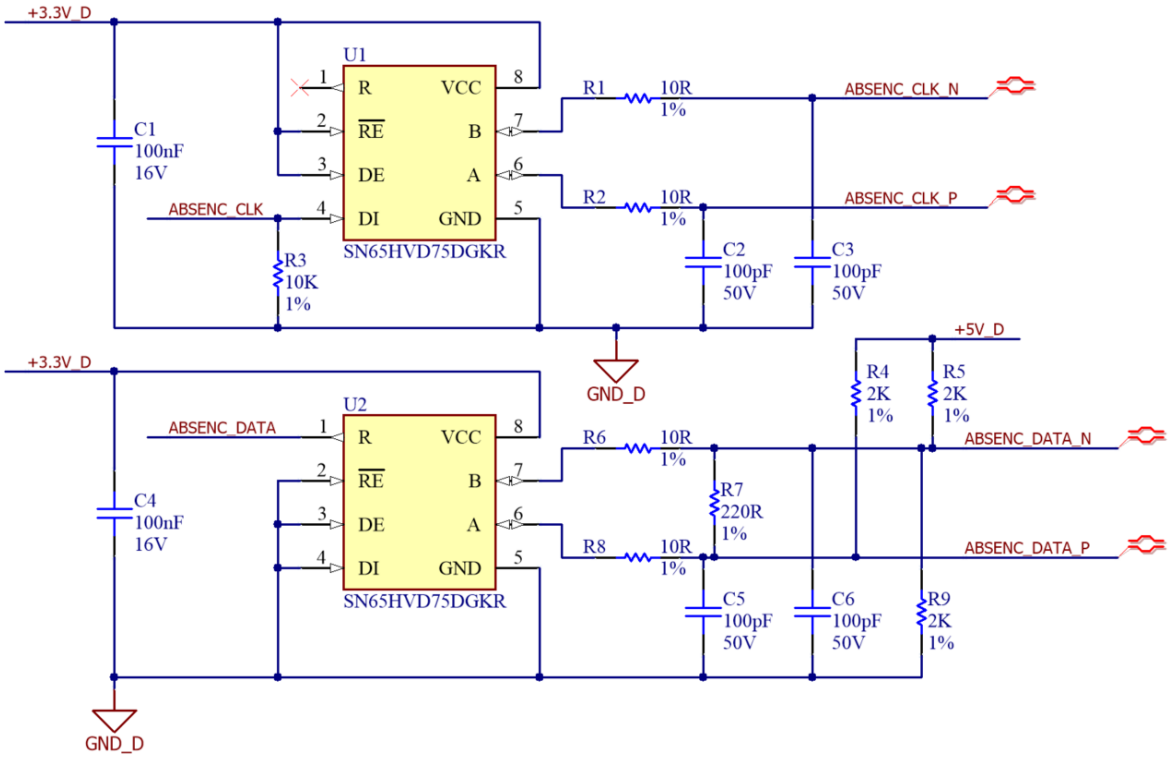
**Bill of materials**

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| C1, C2, C5, C8 | GRM155R71C104KA88D | Murata | 0402 | Ceramic capacitor, 100 nF, 16 V, X7R |
| C3, C4, C6, C7, C9, C10 | CC0402JRNPO9BN101 | Yageo | 0402 | Ceramic capacitor, 100 pF, 50 V, NP0 |
| R1, R2, R6, R7, R8, R12, R13, R14, R18 | RMCF0402FT2K00 | Stackpole | 0402 | Thick film resistor, 2 kΩ, 1 % tolerance, 1/16 W |
| R3, R9, R15 | ERJ3EKF2200V | Panasonic | 0603 | Thick film resistor, 220 Ω, 1 % tolerance, 0.1 W |
| R4, R5, R10, R11, R16, R17 | MC 0.063W 0603 1% 10R | Multicomp | 0603 | Thick film resistor, 10 Ω, 1 % tolerance, 1/16 W |
| U1, U2, U3 | MAX3280EAUK+T | Maxim | SOT-23-5N | Single differential RS422/RS485 line receiver, 52 Mbps, 3 V to 5.5 V supply |

## Absolute Encoder

This circuit is designed to set a RS422/485-based physical layer, which is the most common among absolute encoders. It sets 2 half-duplex channels, one for the "clock" signal, which is always a transmitter driven from the Everest NET, and the other for the "data" signal, which is always a receiver. With this, Everest NET will be able to interface most SSI or BISS-C absolute encoders available.

### Schematic




### Signals description

| Signal | Description |
|---|---|
| +3.3V_D | +3.3 V Logic supply |
| +5V_D | +5 V Logic supply |
| ABSENC_CLK_N | Clock output differential pair to absolute encoder |
| ABSENC_CLK_P | |
| ABSENC_DATA_N | Data input differential pair to absolute encoder |
| ABSENC_DATA_P | |
| ABSENC_CLK | Clock signal from Everest NET to be connected to pin 38 of Feedback connector or pin 24 of Interface connector |
| ABSENC_DATA | Data signal from Everest NET to be connected to pin 40 of Feedback connector or pin 25 of Interface connector |
| GND_D | Logic supply reference voltage. To be connected to pin 36 of Feedback connector or either pins 15, 17 or 35 of Interface connector |

**Design Notes**

- The circuit does not include a termination resistor the Clock output, although it might be advisable if the absolute encoder is connected along a very long cable, or a harsh electromagnetic environment.
- C2, C3, C5 and C6, in combination with R1, R2, R6 and R8, perform a protective function of the transceiver in front of spikes or ESD, and at the same time increases immunity to common mode noise. Capacitors could be increased up to 220 pF to reinforce this effects even more if required.
- If a stronger ESD protection is required, a TVS diodes with capacitance <100 pF are acceptable, whenever C2, C3, C5 and C6 values are kept as suggested.
- The Data receiver uses a resistor voltage divider to set a 2.5 V bias. This would allow connecting this circuit to a single-ended absolute encoder and still being able to read it properly. In this case, leave the negative terminal of the differential pair unconnected.
- R4 pulls-up the positive terminal for an extra robustness in front of a weak and noisy connection.
- C1 and C4 are decoupling capacitors for U1 and U2.

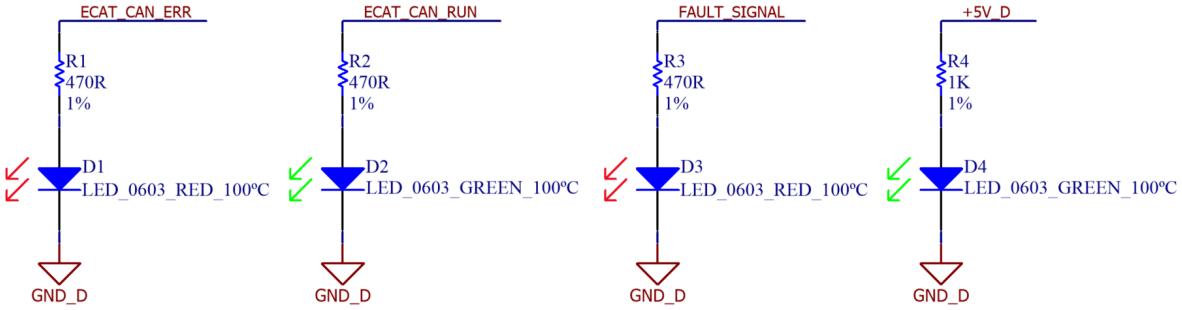
**Bill of materials**

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| C1, C4 | GRM155R71C104KA88D | Murata | 0402 | Ceramic capacitor, 100 nF, 16 V, X7R |
| C2, C3, C5, C6 | CC0402JRNPO9BN101 | Yageo | 0402 | Ceramic capacitor, 100 pF, 50 V, NP0 |
| R1, R2, R6, R8 | MC 0.063W 0603 1% 10R | Multicomp | 0603 | Thick film resistor, 10 Ω, 1 % tolerance, 1/16 W |
| R3 | RMCF0402FT10K0 | Stackpole | 0402 | Thick film resistor, 10 kΩ, 1 % tolerance, 1/16 W |
| R7 | ERJ3EKF2200V | Panasonic | 0603 | Thick film resistor, 220 Ω, 1 % tolerance, 0.1 W |
| R4, R5, R9 | RMCF0402FT2K00 | Stackpole | 0402 | Thick film resistor, 2 kΩ, 1 % tolerance, 1/16 W |
| U1, U2 | SN65HVD75DGKR | Texas Instruments | 8-VSSOP | RS485/422 half-duplex transceiver, 20 Mbps |

### 7.2.7. LED Signalling

Everest NET allows directly driving small LEDs for signalling up to 3 mA. This circuits would provide signalling for EtherCAT / CANopen status signals and Fault signalling of the internal state-machine of the Everest NET.

### Schematic




### Signals description

| Signal | Description |
|---|---|
| +5V_D | +5 V Logic supply for power ON signalling |
| FAULT_SIGNAL | Fault state of the motion controller signalling. To be connected to pin 36 of the Everest NET Interface connector |
| ECAT_CAN_RUN | EtherCAT / CANopen "Run" status signal. To be connected to pin 65 of the Everest NET Interface connector |
| ECAT_CAN_ERR | EtherCAT / CANopen "Error" status signal. To be connected to pin 64 of the Everest NET Interface connector |
| GND_D | Logic supply reference voltage. To be connected to GND_D in the Everest NET Interface connector |

### Design Notes

- In case brighter LEDs are required, **non-inverting** buffers or transistors can be used to increase the output current.
- Also, brightness might substantially vary with this solution, as 3 of the 4 signals carry 3.3 V levels. Using level shifters to 5 V, and re-dimensioning resistors R1, R2 and R3 will notably improve brightness stability.

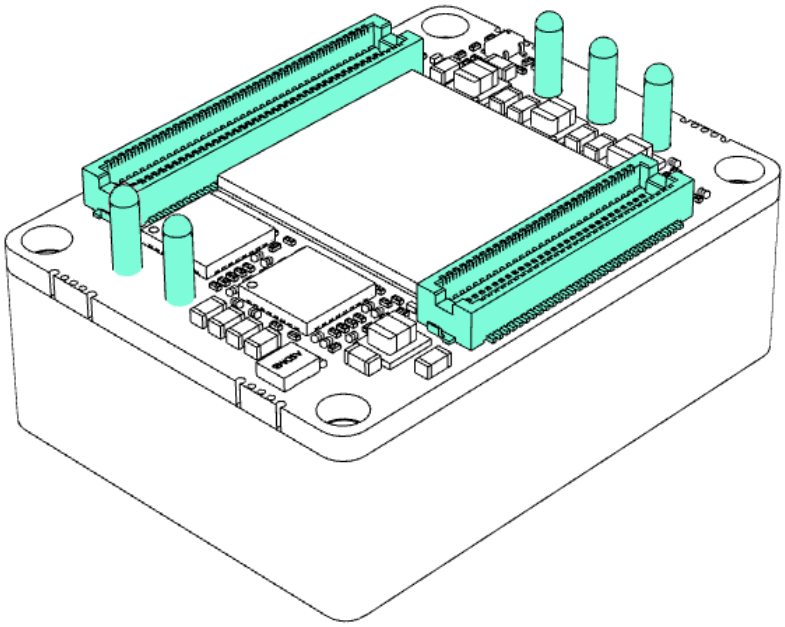
### Bill of materials

| Designator | Part Number | Manufacturer | Package | Value / Description |
|---|---|---|---|---|
| R1, R2, R3 | RC0402FR-07470RL | Yageo | 0402 | Thick film resistor, 470 Ω, 1 % tolerance, 1/16 W |
| R4 | RMCF0402FT1K00 | Stackpole | 0402 | Thick film resistor, 1 kΩ, 1 % tolerance, 1/16 W |
| D1, D3 | TLMS1100-GS08 | Vishay | 0603 | Red diode LED, 63 mcd, 100 ºC |
| D2, D4 | TLMG1100-GS08 | Vishay | 0603 | Green diode LED, 35 mcd, 100 ºC |

### 7.3. Layout Design

This part of the guide is intended to provide the necessary indications to design a PCB in which the Everest NET can be properly integrated.

Everest NET can be interfaced by means of **5 power pins** (4 mm pitch) and **2 mezzanine connectors** (0.5 mm pitch).



While the mezzanine connectors can only be interfaced by means of its matching mating connectors, the power pins can either be **directly soldered to the interface PCB**, or be **plugged into a receptacle mating contact**. The first approach would allow Everest NET to reach its specified nominal phase current, but it will not be possible to unplug it from the interface board. On the other hand, the second approach will be limited to the rated current of the contacts, but allowing the Everest NET to be unplugged if required. Both strategies will require TH pads to hold the Everest NET, meaning that a full footprint for Everest NET would **require mixed assembly technologies, both THT and SMT**.

#### 7.3.1. Required files

To start with, you can download the files linked below:

Atium Project Example

Altium Device Sheet Module

Altium Integrated Library

- **Altium Integrated Library:** contains the symbols and footprints for Everest NET as well as for the required PCB mating connectors, power pin contacts and standoffs.
- **Altium Device Sheet Module:** allows to easily add Everest NET plus all the components required to plug it to an Altium project.
- **Altium Project Example:** simple Altium project template where the Everest NET module has already been added to schematic and PCB.

### 7.3.2. The Everest NET component

The Everest NET is not directly plugged to a PCB, but instead it uses components to be plugged to, either along the direct solder or the pluggable approach. This components are:

- **Standoffs:** SMD standoffs are preferred in front of traditional standoffs, as once soldered they cannot move, thus making easier to respect the small clearances to surrounding copper or components.
- **Signal connectors:** 60-pin and 80-pin mezzanine male mating connectors (see **Pinout** section for more info).
- **Power pin receptacles:** mating terminals for pluggable approach or TH holes for soldered approach. Both are disposed as independent components, yet the holes do not entail any BOM (only copper).

> **Plugged vs. Soldered approach**
> Pluggable approach would require terminals P1, P2, P3, P4 and P5, while soldered approach would require holes H1, H2, H3, H4 and H5. In the Device Sheet Module attached both sets of elements are superposed in the PCB (this might be shown as a component clearance conflict). Whichever is the selected approach, remove the components for the other from schematic, and update the PCB. When only 1 of the 2 sets of components remain in the PCB, the conflict should be gone.

Notice this means that the Everest NET component does not have any terminals nor copper in its footprint. The copper comes from the mating and fixing elements listed above. However, the PCB component does include some critical information in various of its mechanical layers:

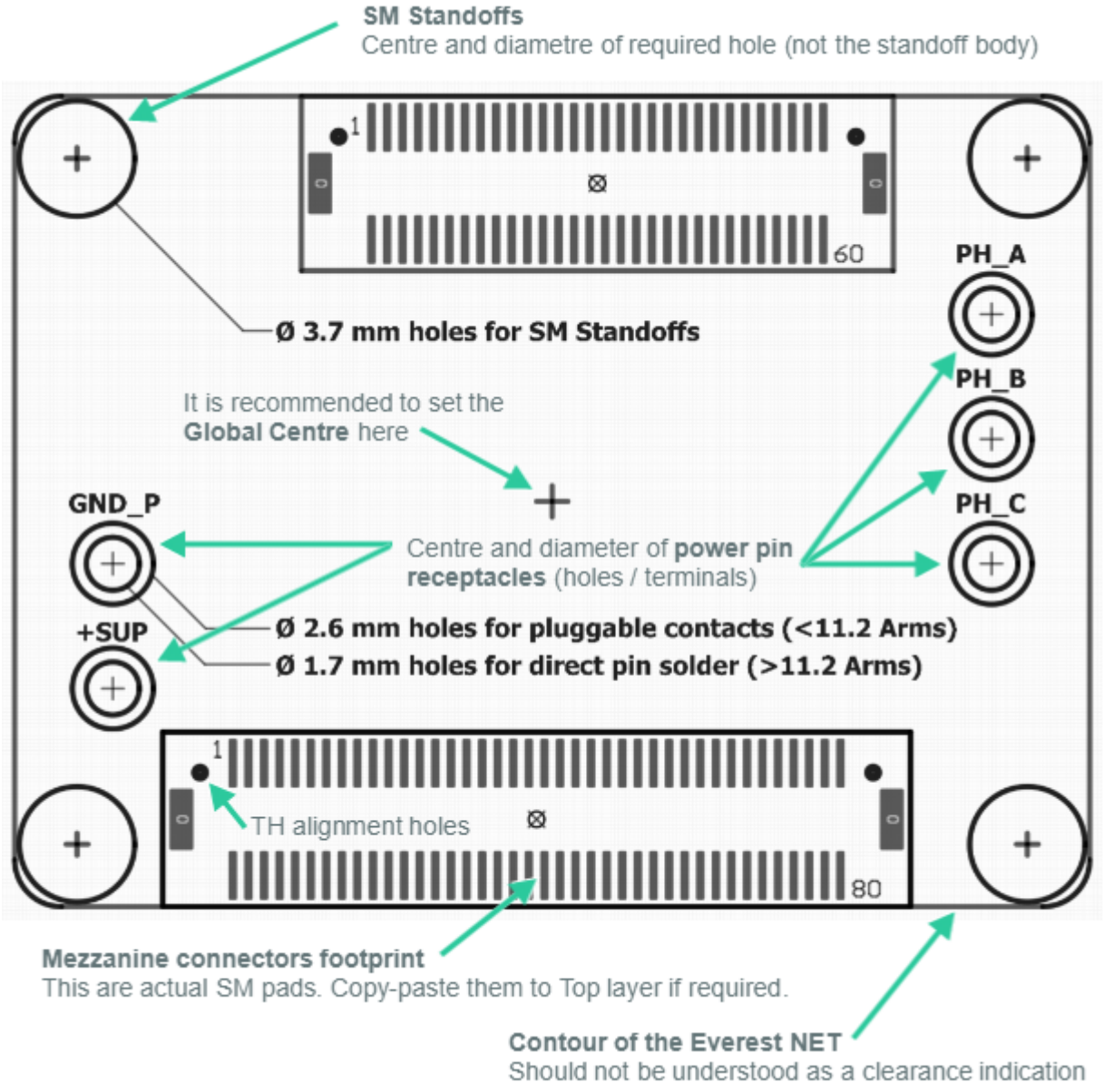
- **Mechanical layer 5:** can be used as a positioning guide for the required mating and fixing elements.
- **Mechanical layer 10:** contains the bounding boxes and designators for each component, used to generate the Assembly Drawing 2D output. If the Everest NET is flipped from Top to Bottom layer, this information should move to Mechanical layer 11, according to the defined layer pairs this component has been created with.

- **Mechanical layer 13:** contains the 3D body of Everest NET in a native STEP AP214 format (STEP file alone can be downloaded from the **Dimensions** section).
- **Mechanical layer 15:** contains critical information on clearances to nearby components, as well as routing considerations.

### Mechanical layer 5: positioning guide

This mechanical layer contains useful mechanical data, including the centre of all the mating and fixing components, as well as their diameters or bounding boxes. It also includes a full footprint representation of the 2 mezzanine connectors, plus their proper orientation with first and last pins marked.

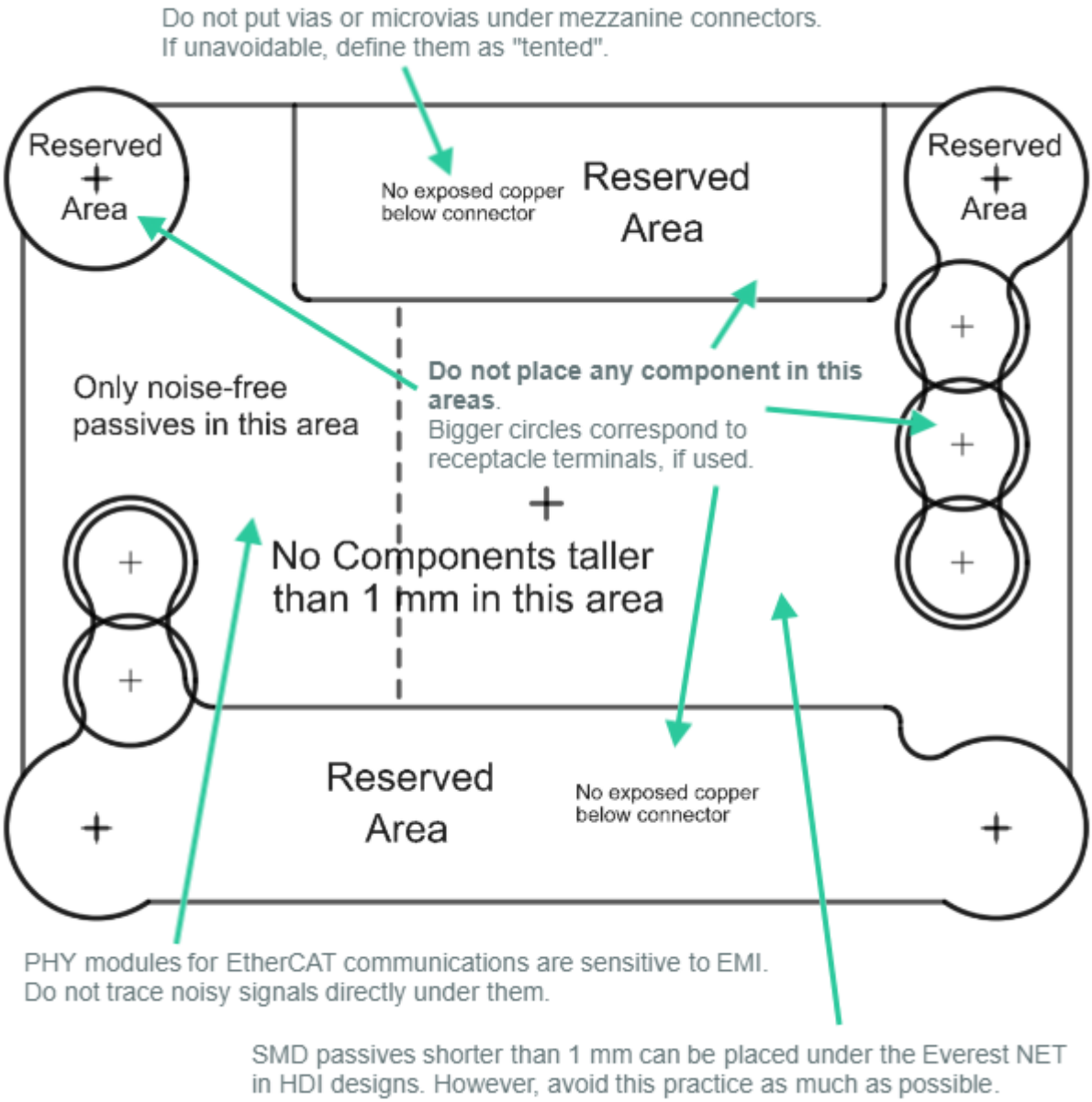
> **Footprint of mezzanine connectors**
> Mechanical 5 includes the footprint of the 2 required mating mezzanine connectors. It is not made out of rectangular shapes representing copper, but actual numbered SM and TH pads. Therefore, to generate a footprint for the mezzanine connectors, simply copy all the pads from Mechanical layer 5, and paste them into Top layer.



Comfortably, drag-and-drop the mating and fixing components referenced to their respective centres to the centre positions marked in Mechanical 5. Do this carefully to avoid an excessive mechanical stress to the Everest NET when plugged into the PCB.

### Mechanical layer 15: clearances

Considerations about clearances and general layout advice can be found in Mechanical layer 15. Understand the lines as the limits for component placement outside or below the Everest NET, in such way that no component should cross them.

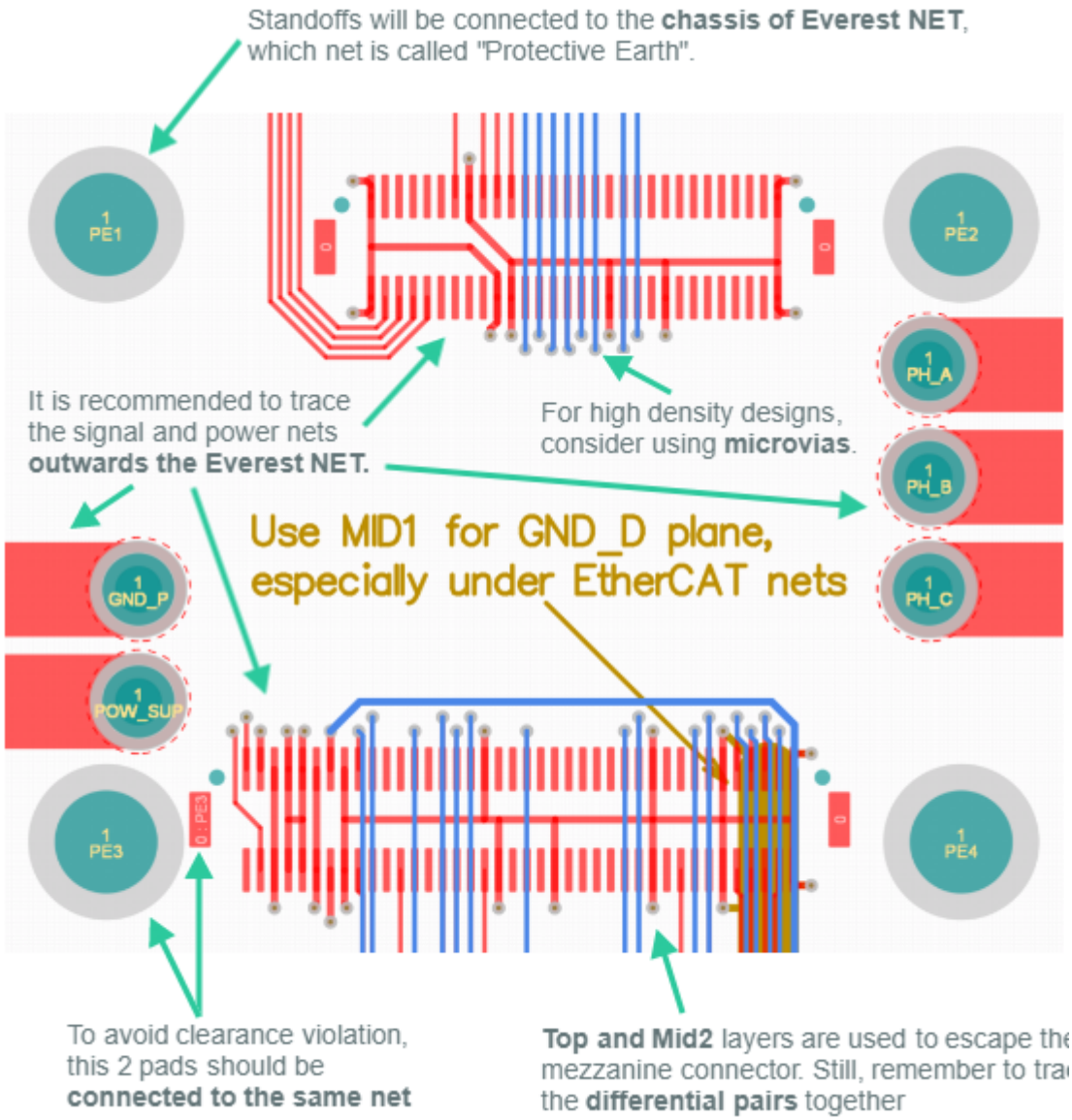



HDI designs with strong size constraints can benefit from placing components directly under the Everest NET, whenever they are **under 1 mm height**. However, this has to be done very carefully, not only with a total certainty on the height of the component and its tolerance, but also discarding any trace or component that could become both an "aggressor" or "victim" from the EMC point of view. This is specially important under the PHY modules, as the whole EtherCAT communications could be affected by a nearby radiating trace or a capacitive coupling.

As an example, to not lay the copper connected to the power pins towards the inside of the Everest NET, but towards the outside. This would prevent the power signals from affecting sensitive circuits of the Everest NET.

### 7.3.3. Layout considerations

The attached snippet includes the footprints of the mating and fixing components, as well as a basic layout proposal. Only signal traces are represented, with the purpose of pointing the most appropriate way of leaving the Everest NET. As a rule of thumb, it is preferred to not direct the layout towards the inside of the Everest NET, but outwards.




In the proposed layout, copper in Top layer is represented in red, Mid layer 1 is represented in yellow and Mid layer 2 in blue (some traces might be hidden in the image). This proposal also uses simple TH vias sized to fit a very attainable Class 6 PCB manufacturing category. This is a quite average level of sophistication, in terms of PCB manufacturing technology, but is sufficient to interface the Everest NET, thus entailing a cheaper cost. However, very dense designs might go for a less restrictive PCB Class, specially when most of the signals in the mezzanine connectors are used.

**Use of vias or microvias**
Although not specifically required, designs where most of the signal pins are used at the same time may consider interfacing the mezzanine connectors with microvias between Top and Mid 1 layers instead of classical TH vias. Note that this might entail higher PCB manufacturing costs.

**GND_D below EtherCAT tracks**
It is highly recommended to reserve the whole Mid 1 layer to set a copper plane connected to GND_D; this is of an special importance in the area that is directly below and over the EtherCAT tracks going through Top and Mid 2 layers. This way, a low inductance return path is guaranteed to minimise any possible EMC issue.
But in the event there is no possible way to set this continuous GND_D plane along the EtherCAT tracks path, be sure to not overlap any of the 4 differential pairs along directly adjacent layers: this could cause a substantial cross-talk due to capacitive coupling, which can lead to serious malfunction of the communications. On the other hand, overlapping the positive and negative tracks of the same differential pair along directly adjacent layers is might be acceptable.

### Proposed Layer Stack

Although many other options may be valid, here this 6-layer stack is proposed considering that is pretty standard, and targets the lowest PCB manufacturing cost to allow routing the Everest NET comfortably. The resulting PCB should be around 1.6 mm thick.

| # | Name | Material | Type | Weight | Thickness | Dk | # | Thru 1:6 |
|---|---|---|---|---|---|---|---|---|
| | Top Overlay | | Overlay | | | | | |
| | Top Solder | Solder Resist | Solder Mask | | 0,01mm | 3,5 | | |
| 1 | Top Layer | | Signal | 1oz | 0,035mm | | 1 | |
| | Dielectric1 | FR-4 | Prepreg | | 0,13mm | 4,8 | | |
| 2 | Mid-Layer 1 | | Signal | 2oz | 0,07mm | | 2 | |
| | Dielectric2 | FR-4 | Core | | 0,35mm | 4,8 | | |
| 3 | Mid-Layer 2 | | Signal | 2oz | 0,07mm | | 3 | |
| | Dielectric3 | FR-4 | Prepreg | | 0,22mm | 4,8 | | |
| 4 | Mid-Layer 3 | | Signal | 2oz | 0,07mm | | 4 | |
| | Dielectric4 | FR-4 | Core | | 0,35mm | 4,8 | | |
| 5 | Mid-Layer 4 | | Signal | 2oz | 0,07mm | | 5 | |
| | Dielectric5 | FR-4 | Prepreg | | 0,13mm | 4,8 | | |
| 6 | Bottom Layer | | Signal | 1oz | 0,035mm | | 6 | |
| | Bottom Solder | Solder Resist | Solder Mask | | 0,01mm | 3,5 | | |
| | Bottom Overlay | | Overlay | | | | | |

Note that internal layers are defined as 70 µm copper thickness. When targeting the nominal phase current of Everest NET this would help minimising the number of layers required to carry the phase currents without causing considerable losses due to self-heating. However, this might entail jumping from PCB Class 6 to Class 7 in some cases. Consult your PCB manufacturer. Also, in very small designs where the phases copper self-heating cannot be easily evacuated, consider selecting FR-4 dielectrics with higher glass transition temperatures: Tg = 150 ºC or even Tg = 180 ºC.

As for the example provided, the following usage of each layer is suggested:

| Layer | Purpose |
|---|---|
| Top | Components, signal tracks, GND |
| Mid 1 | GND_D copper plane |
| Mid 2 | Signal tracks, GND |

| Layer | Purpose |
|---|---|
| Mid 3 | Power supplies |
| Mid 4 | Signal tracks, GND |
| Bottom | Components, signal tracks, GND |

**If using µvias**
For higher density designs using µvias from Top to Mid 1, it is recommended to switch the purpose of Mid 1 and Mid 2, tracing the signal tracks along Mid 1 and reserving Mid 2 to set a ground plane connected to GND_D.

### Proposed Design Rules

Again, many options are plausible here, but consider this specific set of rules as the minimum required to integrate the Everest NET without entailing an additional handicap.

| Rule | Value |
|---|---|
| Minimum clearance to Power conductors (external layers) | 0.5 mm |
| Minimum clearance to Protective Earth (chassis) | 0.5 mm |
| Minimum distance between Signal conductors (internal & external layers) | 0.15 mm |
| Minimum track width (internal & external layers) | 0.15 mm |
| Minimum component body clearance | 0.2 mm |
| Minimum annular ring (internal & external layers) | 0.15 mm |
| Minimum plated hole diameter | 0.2 mm |
| Hole to hole clearance | 0.3 mm |
| Paste mask expansion | 0 mm |
| Solder mask expansion | 0.05 mm |
| Minimum solder mask sliver | 0.07 mm |

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